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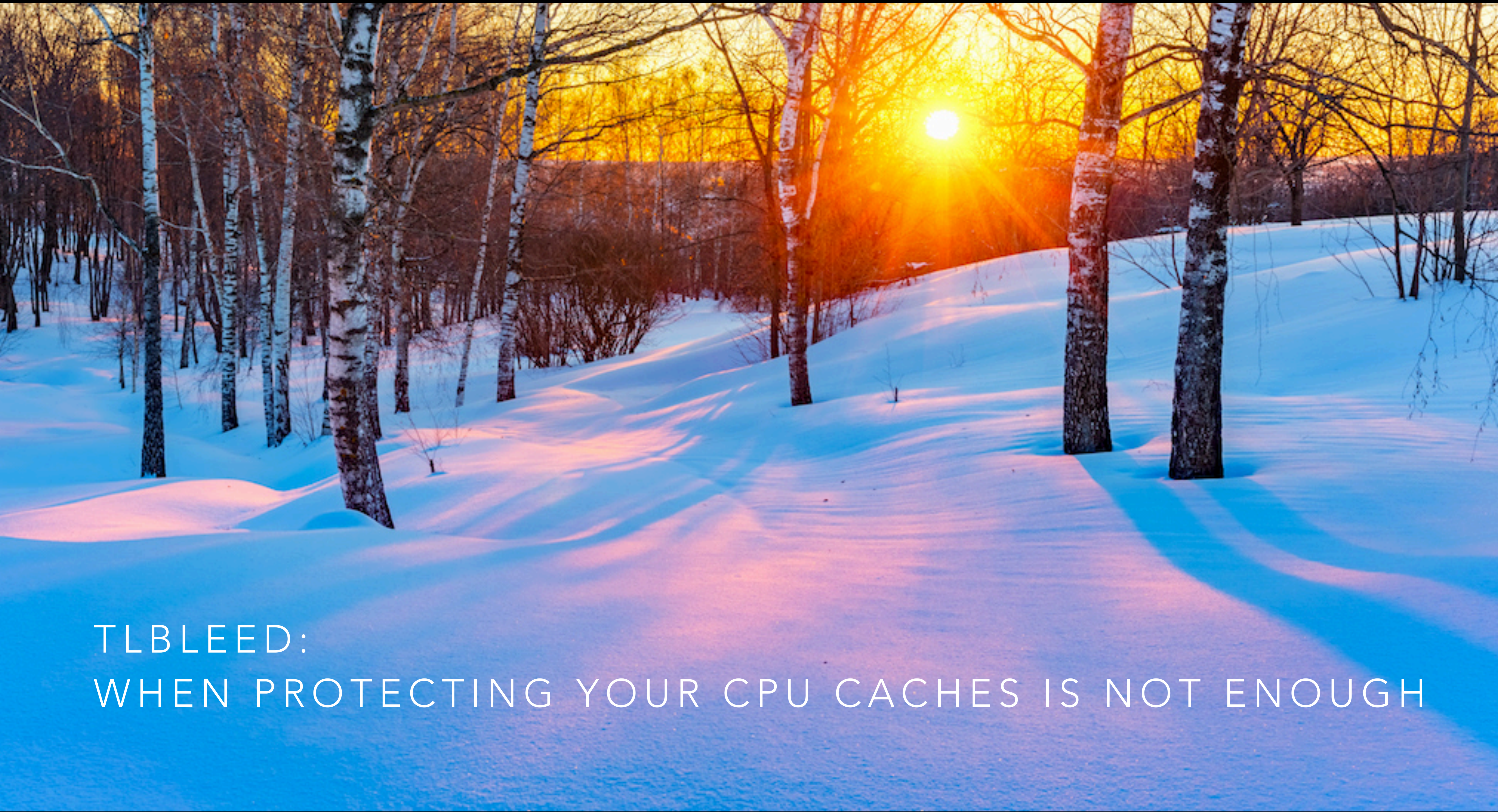
CRISTIANO GIUFFRIDA, HERBERT BOS
VRIJE UNIVERSITEIT AMSTERDAM

HARDWEAR.IO 2018



TLBLEED: WHEN PROTECTING YOUR CPU CACHES IS NOT ENOUGH

ABOUT US

VUSec

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- VUsec - Security Research group at VU Amsterdam

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- Academic group researching systems software security

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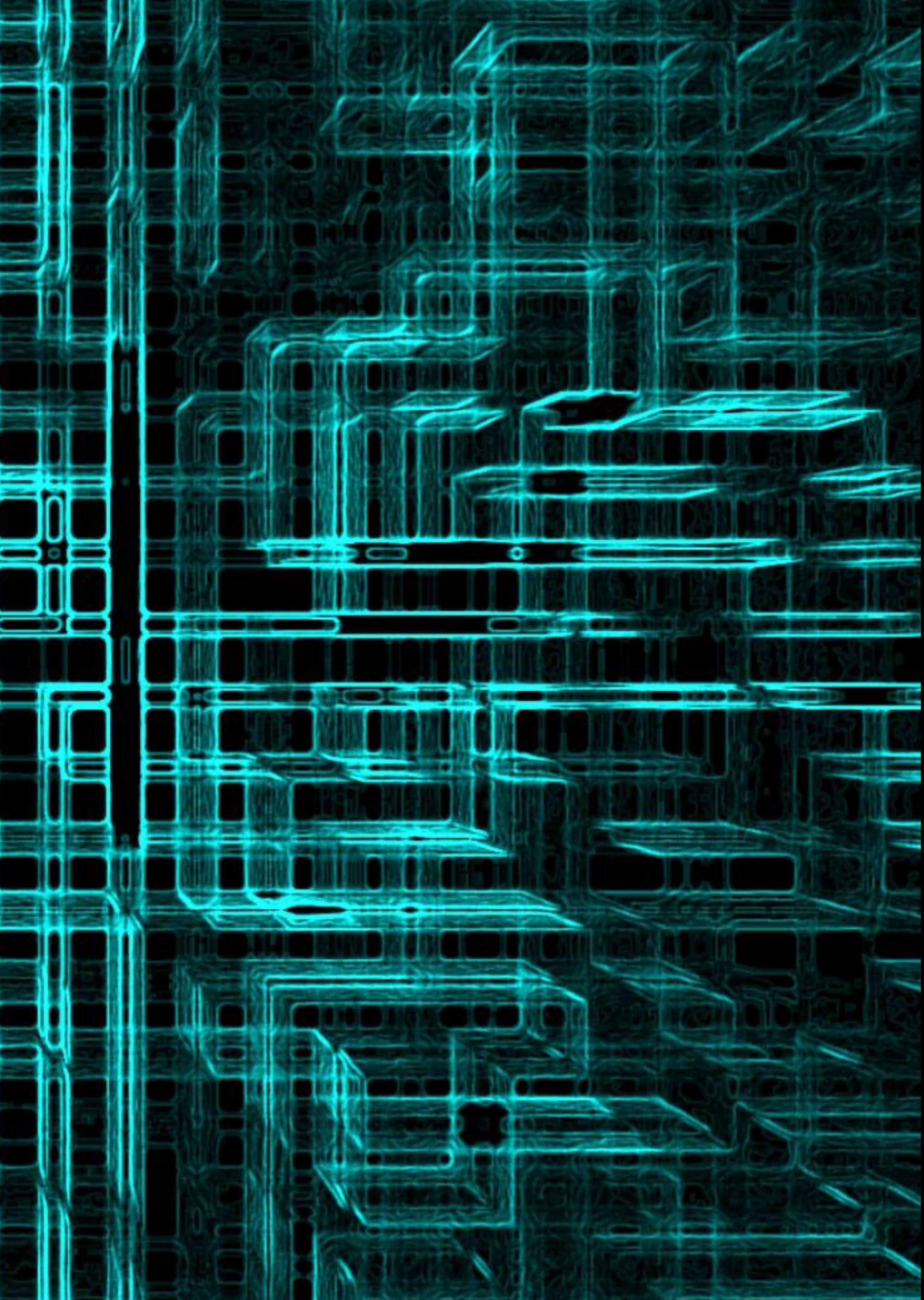
OVERVIEW

- Cache attacks
- Cache defences
- TLBleed
- Evaluation
- Reception



CACHE ATTACKS

SIDE CHANNELS

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- Leak secrets outside the regular interface

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INSIDE A CPU

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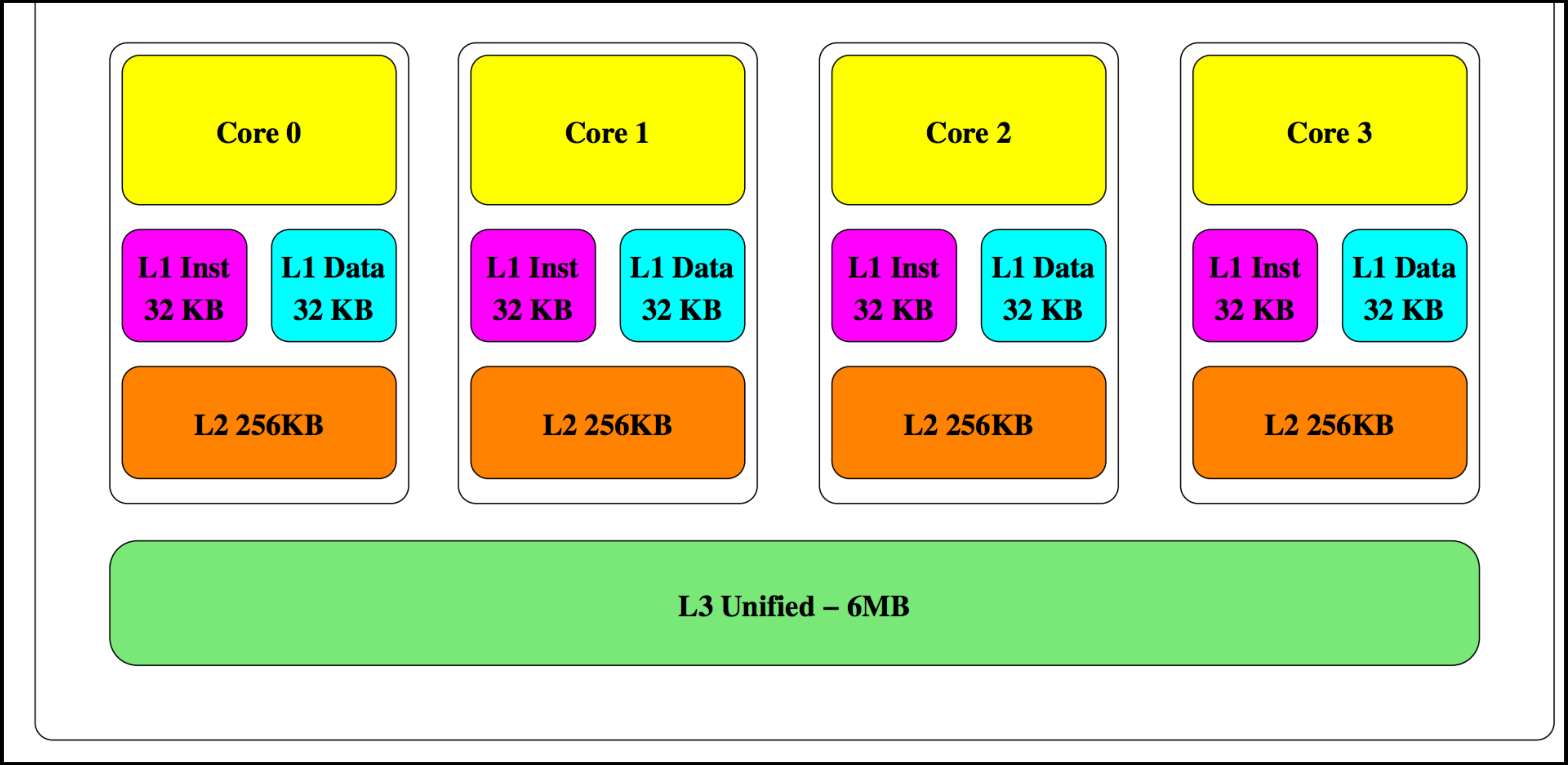
Core 0
L1 Inst 32 KB
L1 Data 32 KB
L2 256KB
Core 1
L1 Inst 32 KB
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L2 256KB
Core 2
L1 Inst 32 KB
L1 Data 32 KB
L2 256KB
Core 3
L1 Inst 32 KB
L1 Data 32 KB
L2 256KB
L3 Unified – 6MB

SIDE CHANNEL ATTACKS ON SHARED RESOURCES

- There are **shared** resources between processes
- RAM, CPU cache, TLB, computational resources ..
- Covert channels
- Sometimes: Side channels (spying)

EXAMPLE: FLUSH+RELOAD

- Work by Yuval Yarom, Katrina Falkner

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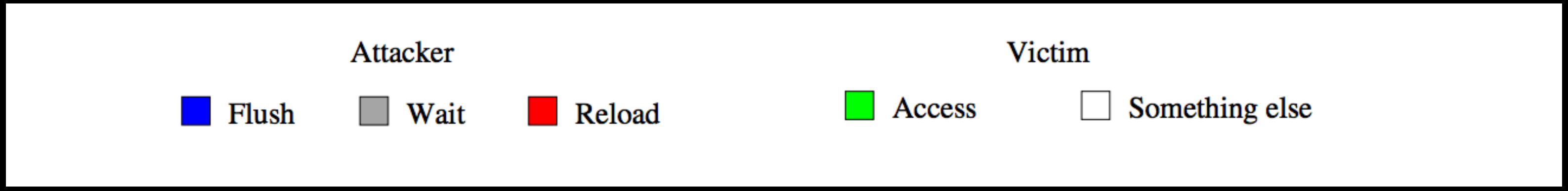

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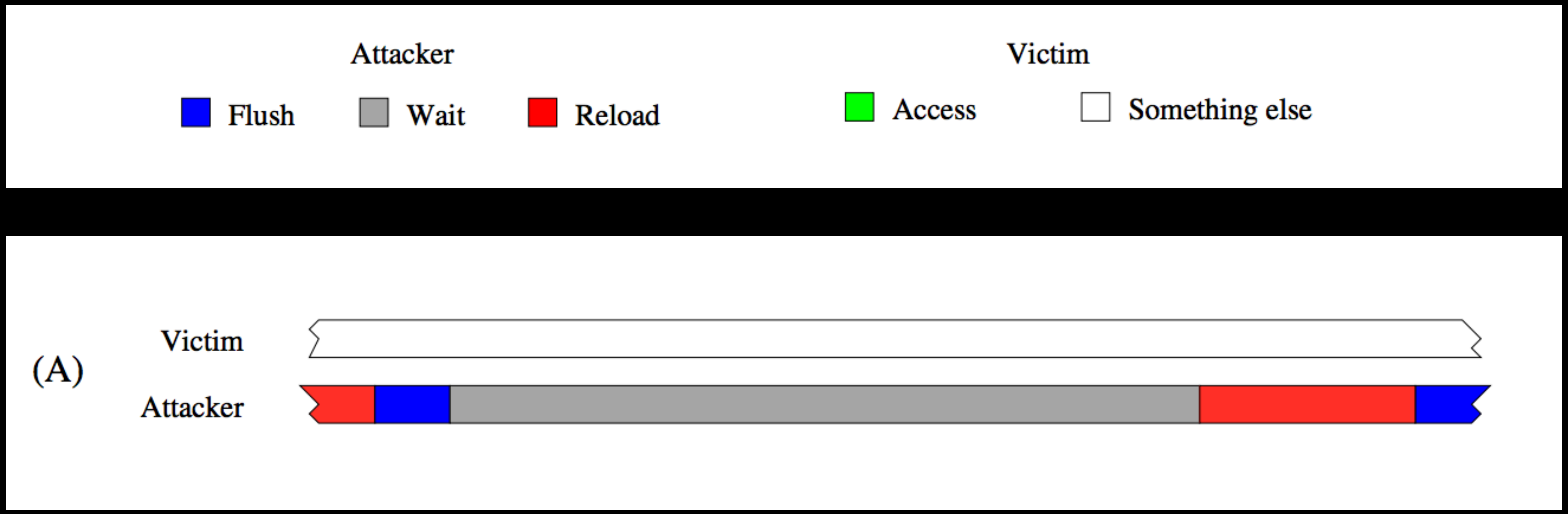

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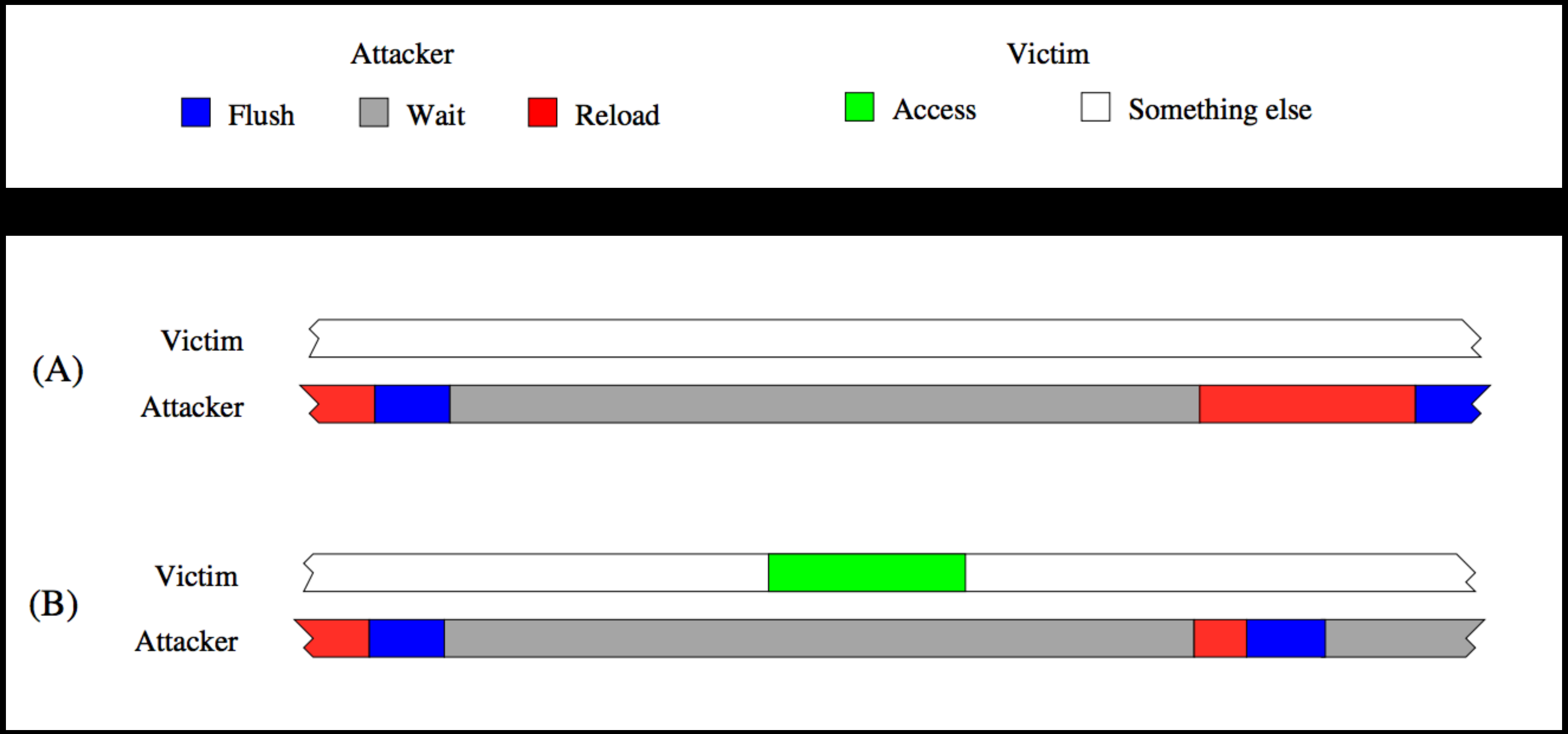

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EXAMPLE: FLUSH+RELOAD

- Can attack AES implementation with T tables
- A table lookup happens $T_j\,[x_i = p_i \oplus k_i\,]$
- p_i is a plaintext byte, k_i a key byte

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- Again: secrets are betrayed by memory accesses
- Known plaintext + accesses = key recovery

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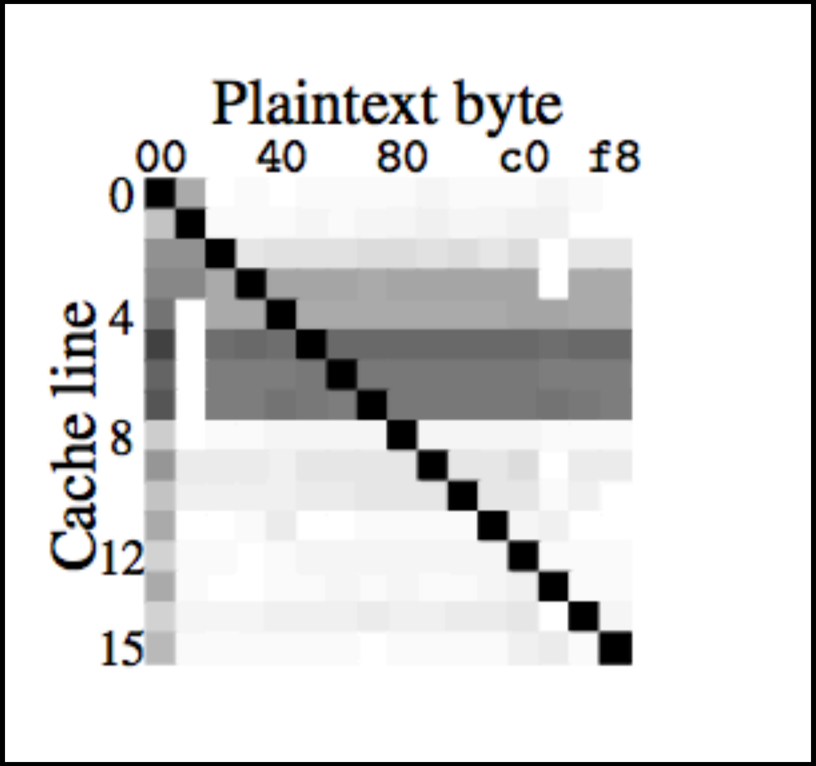

EXAMPLE: LIBGCRYPT ECC

- Not side channel proof version:

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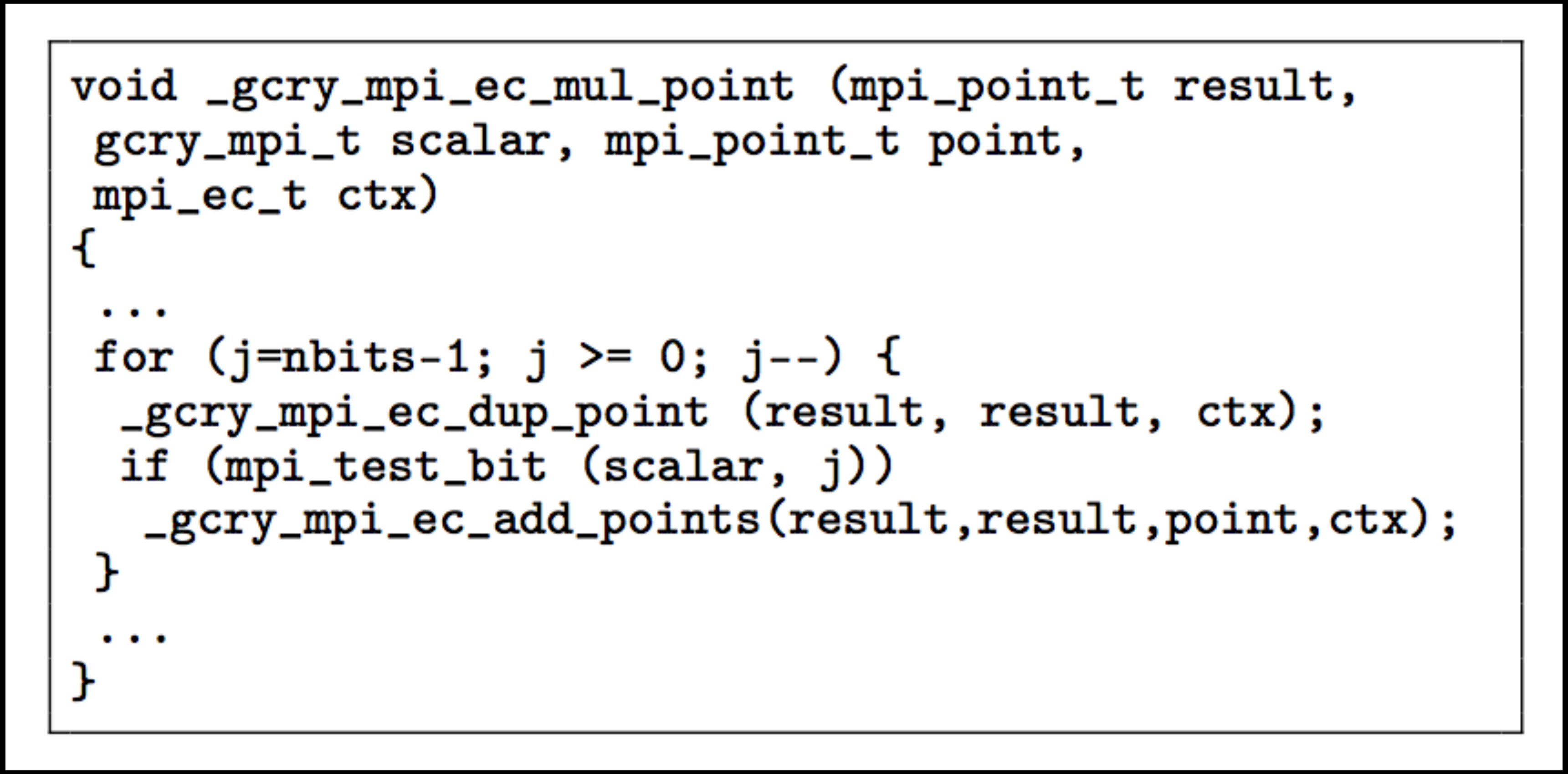

```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
 gcry_mpi_t scalar, mpi_point_t point,
 mpi_ec_t ctx)
{
 ...
 for (j=nbits-1; j >= 0; j--) {
  _gcry_mpi_ec_dup_point (result, result, ctx);
  if (mpi_test_bit (scalar, j))
   _gcry_mpi_ec_add_points(result,result,point,ctx);
 }
 ...
}
```

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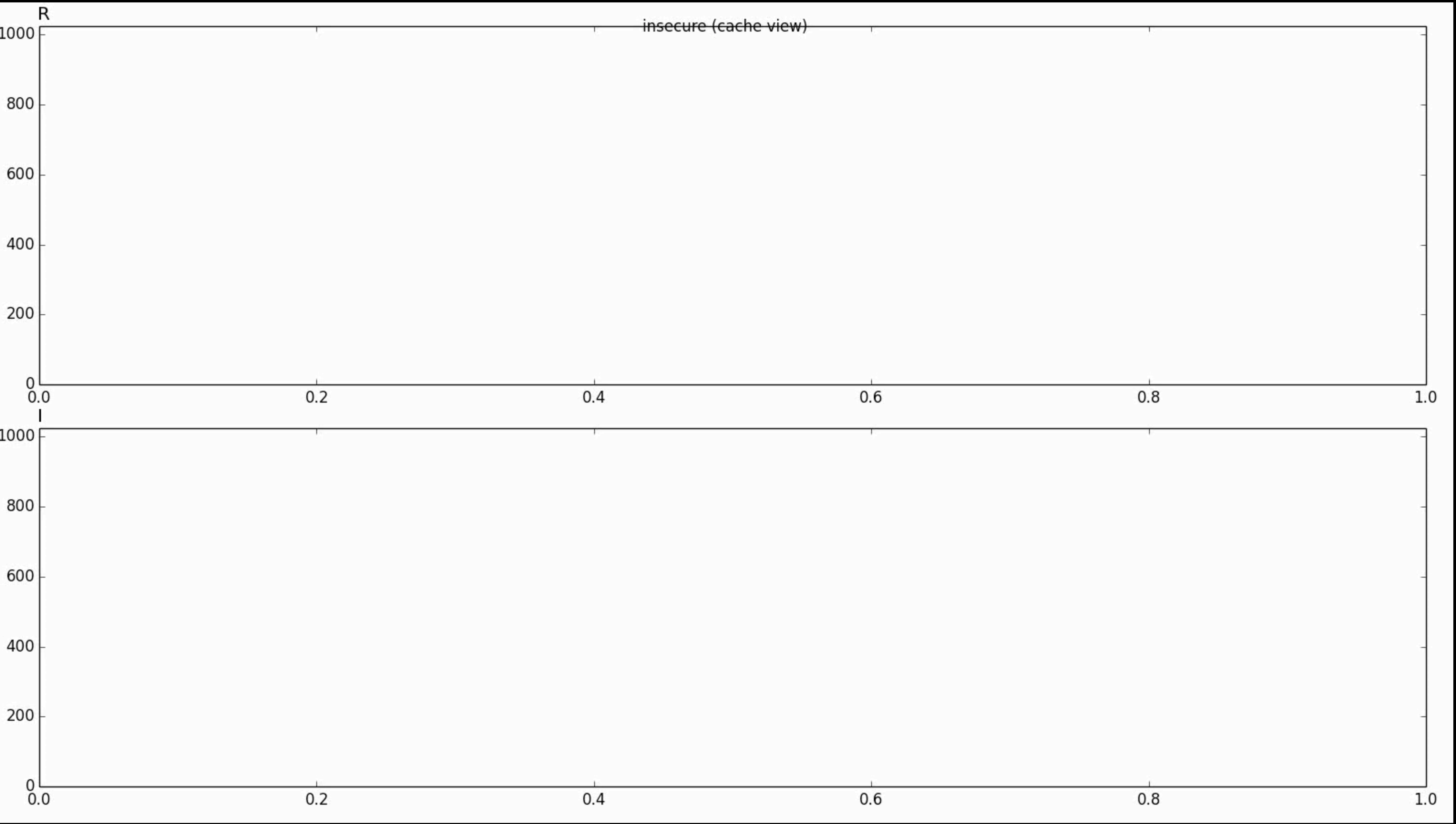

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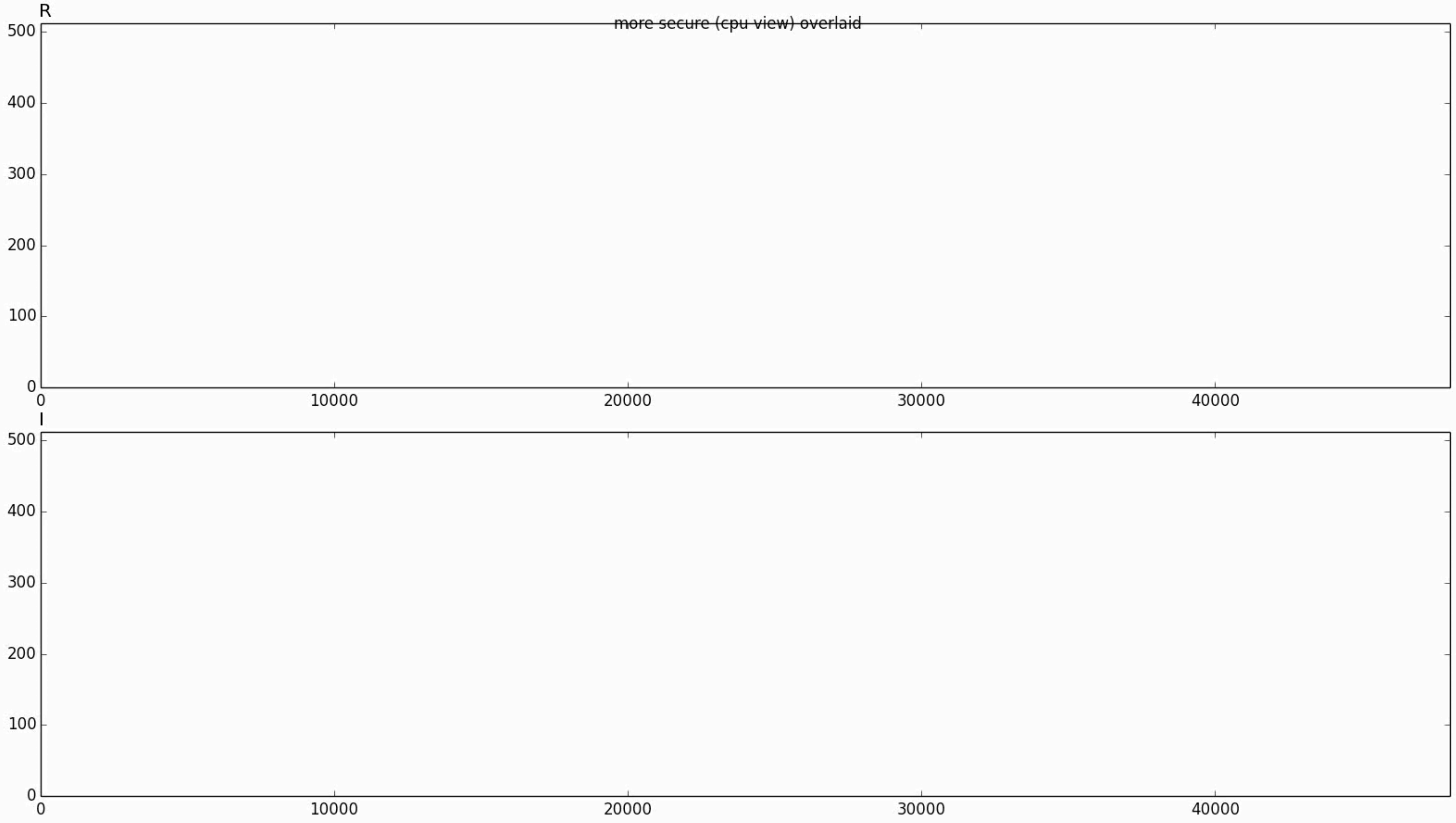
- More side channel proof version

EXAMPLE: LIBGCRYPT ECC



CACHE DEFENCES

CACHE PARTIONING

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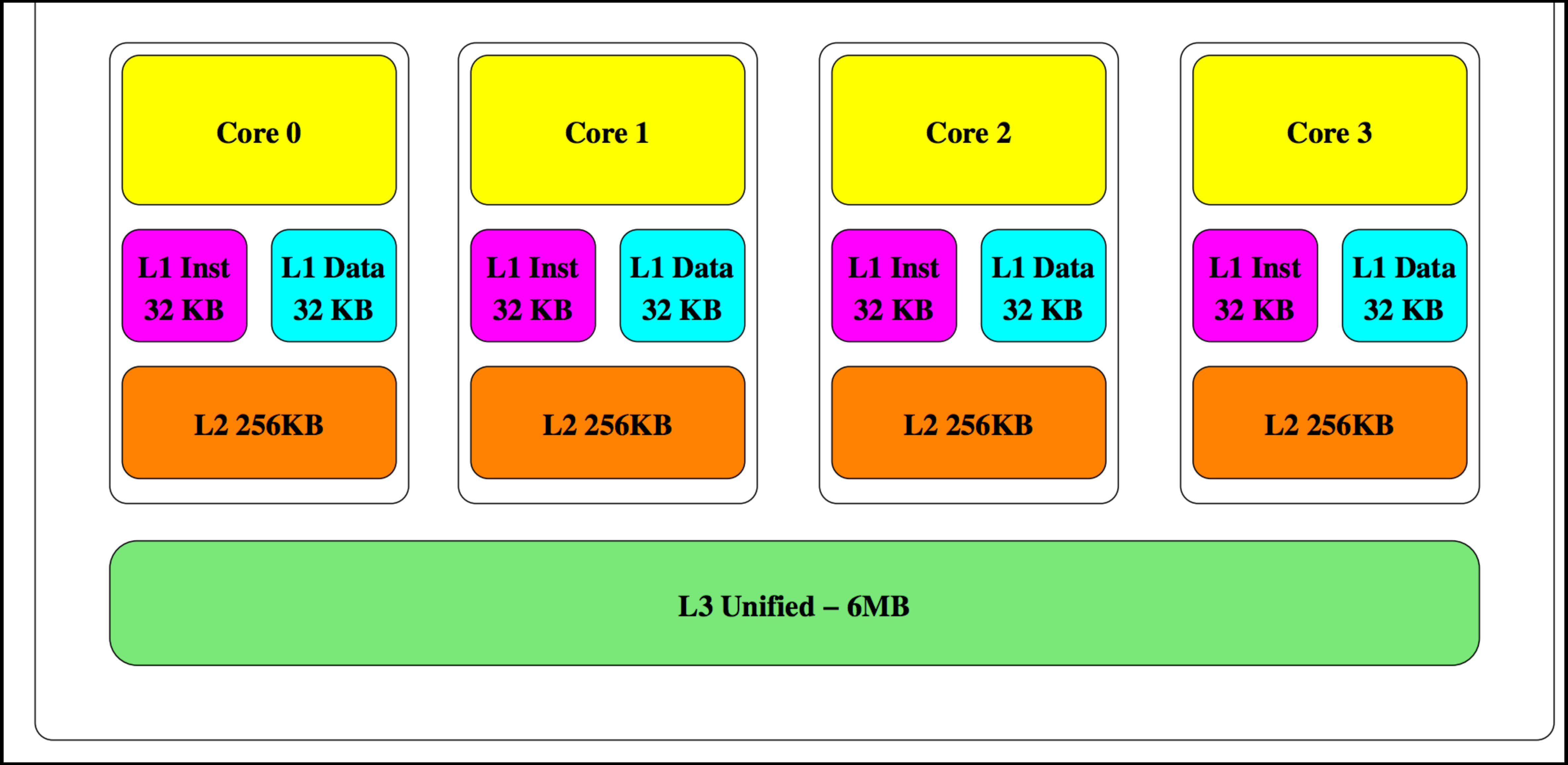
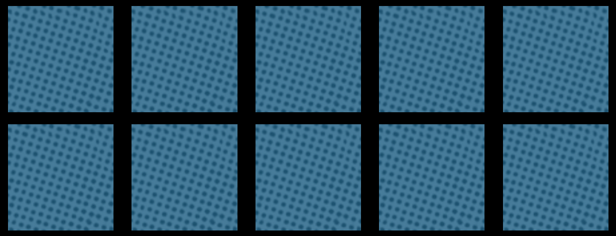


CACHE COLOURING

- Figure out page colors
- These map to shared cache sets
- Do not share same colors across security boundaries
- Kernel arranges this



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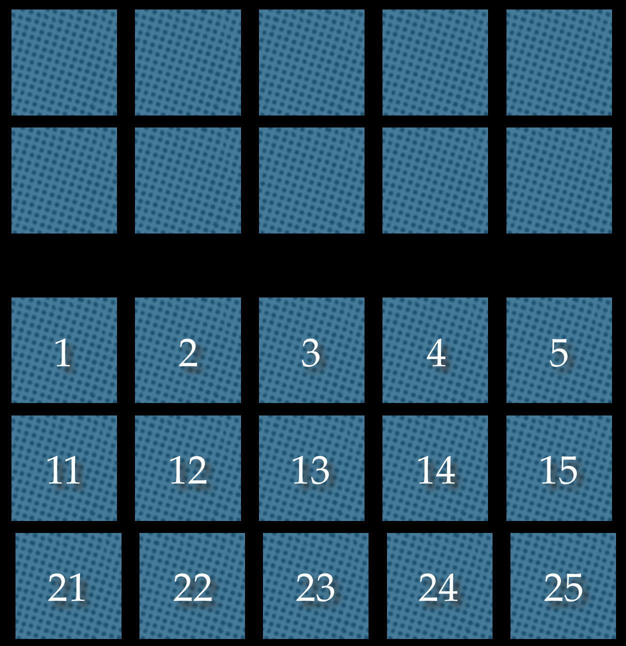

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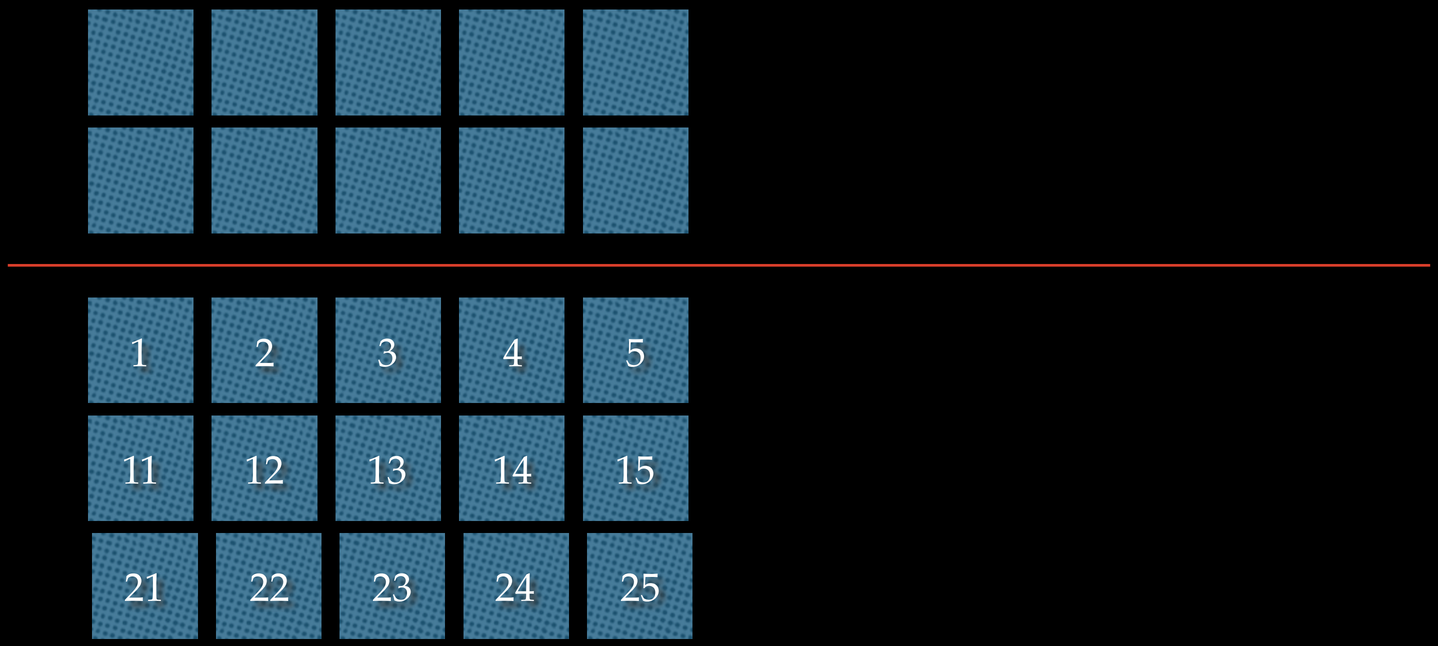

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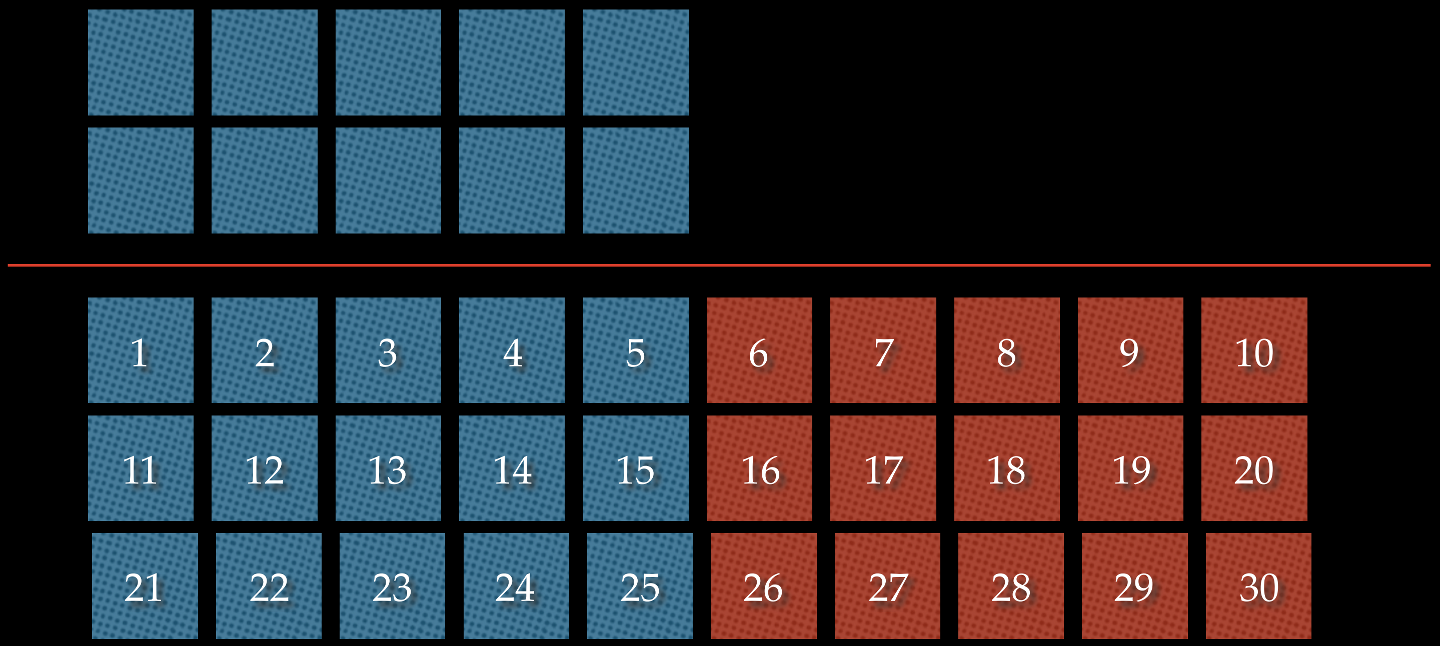

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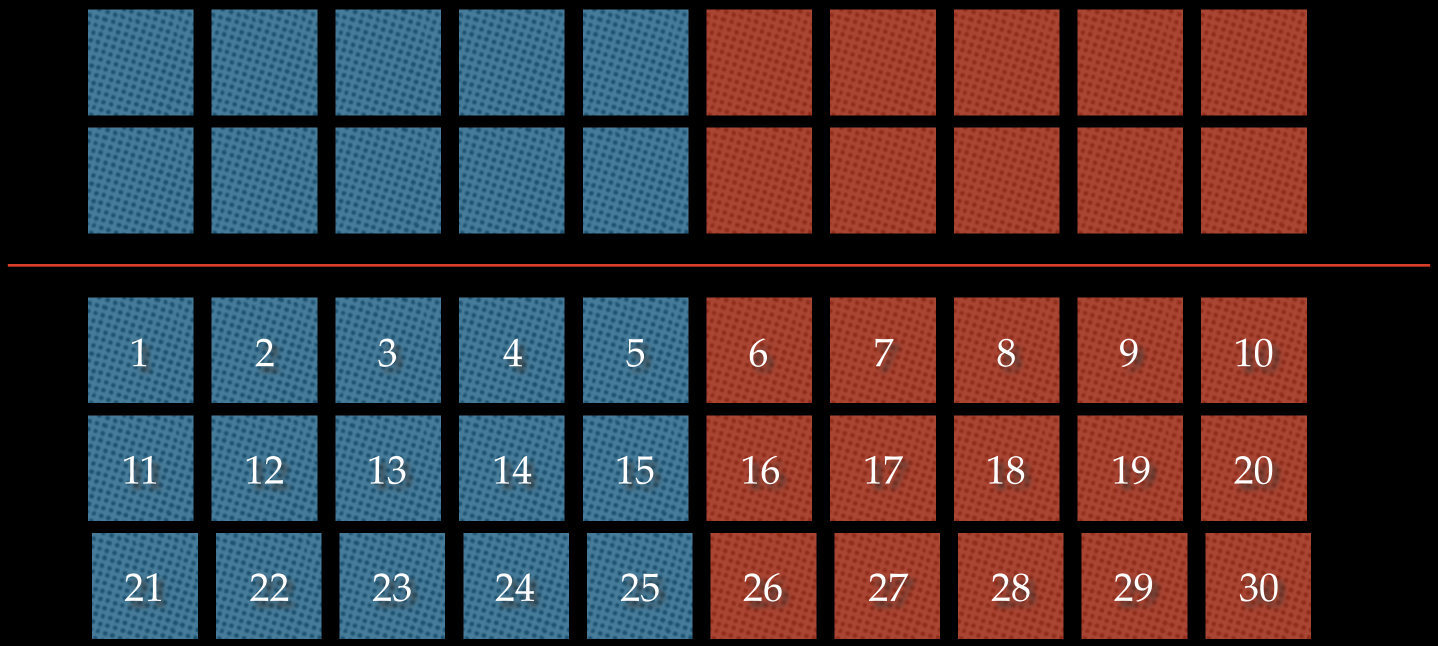

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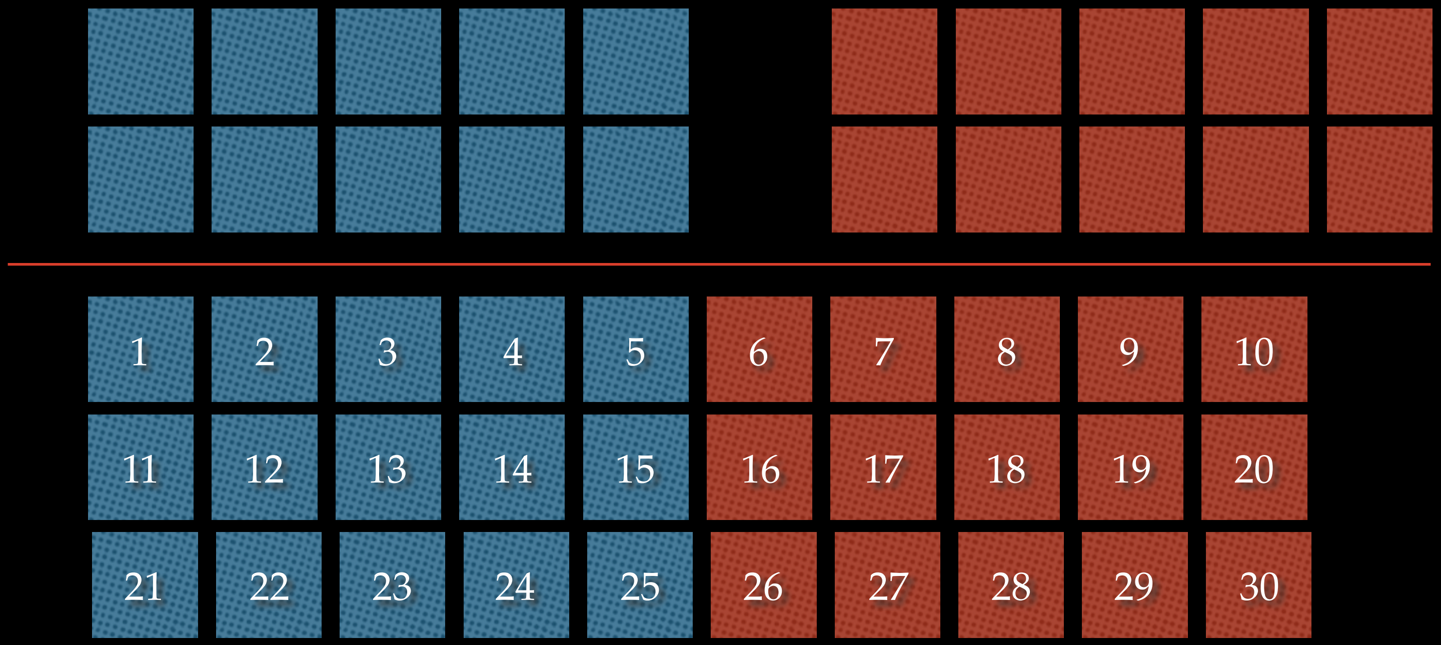

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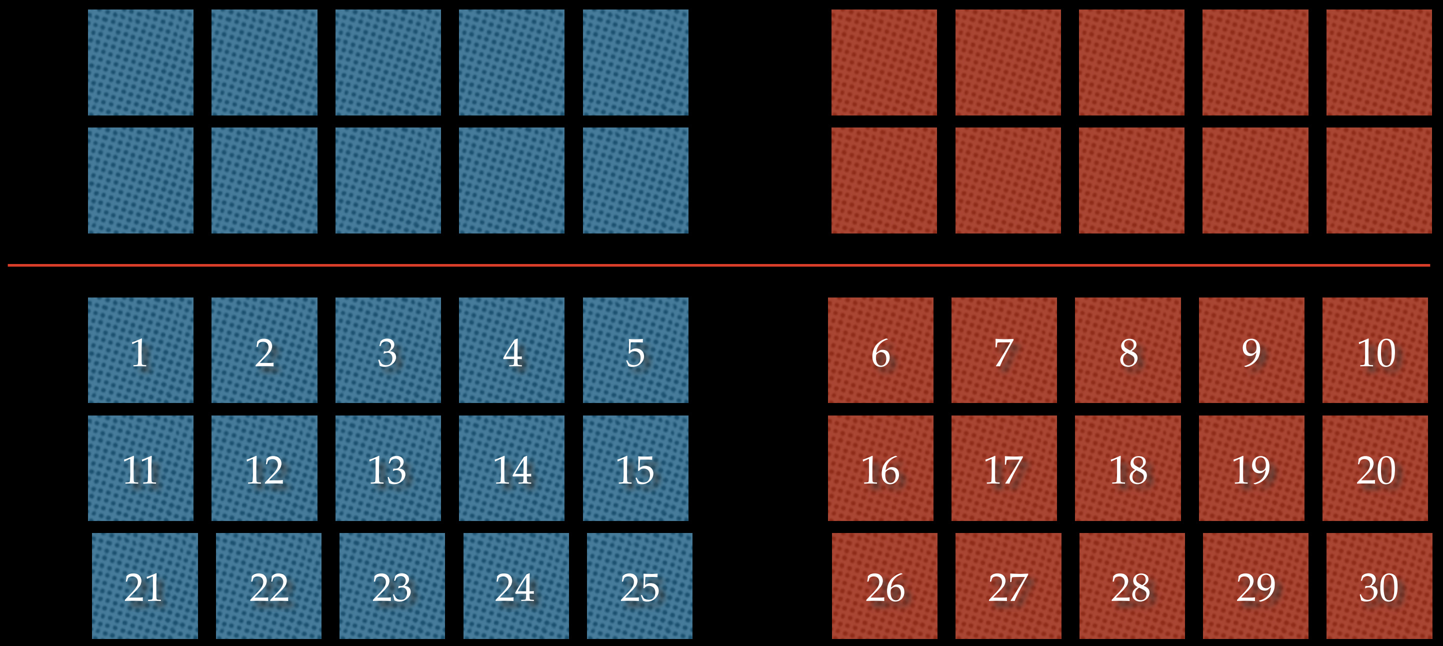

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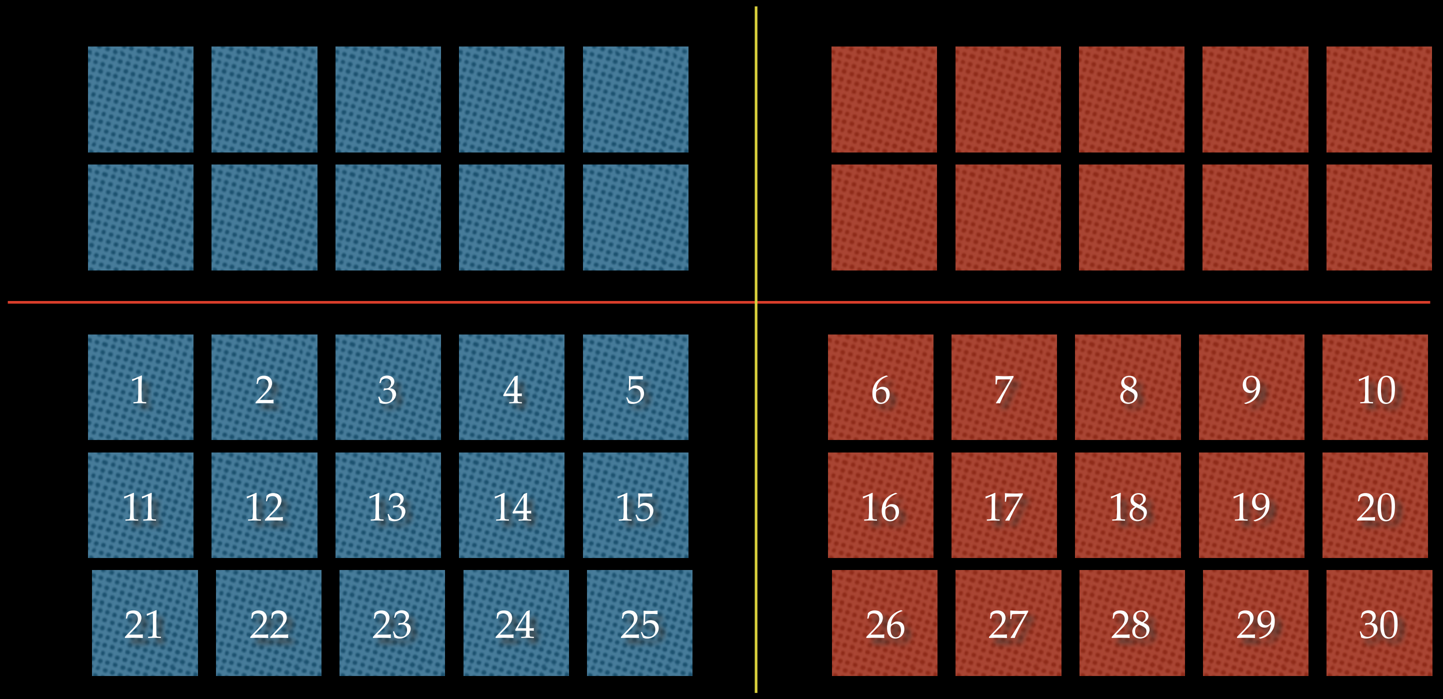

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- Intel CAT: Cache Allocation Technology
- Intended for predictable performance for VMs
- Partitions caches in *ways*
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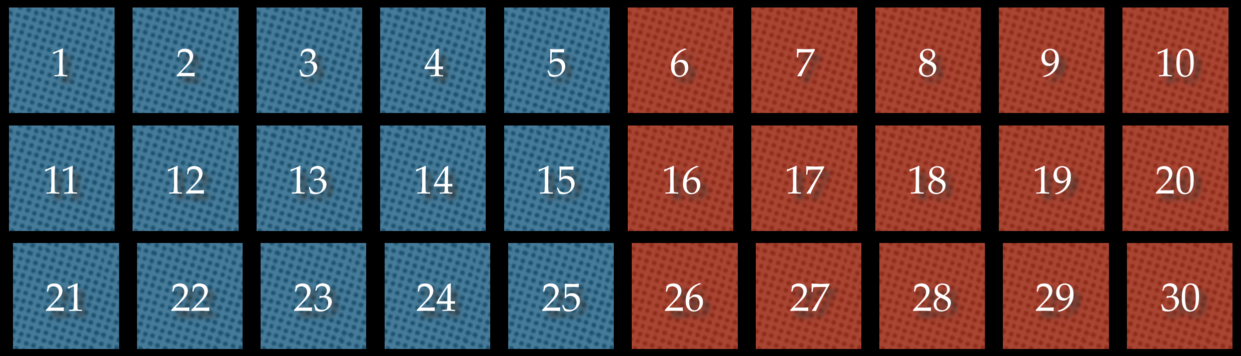

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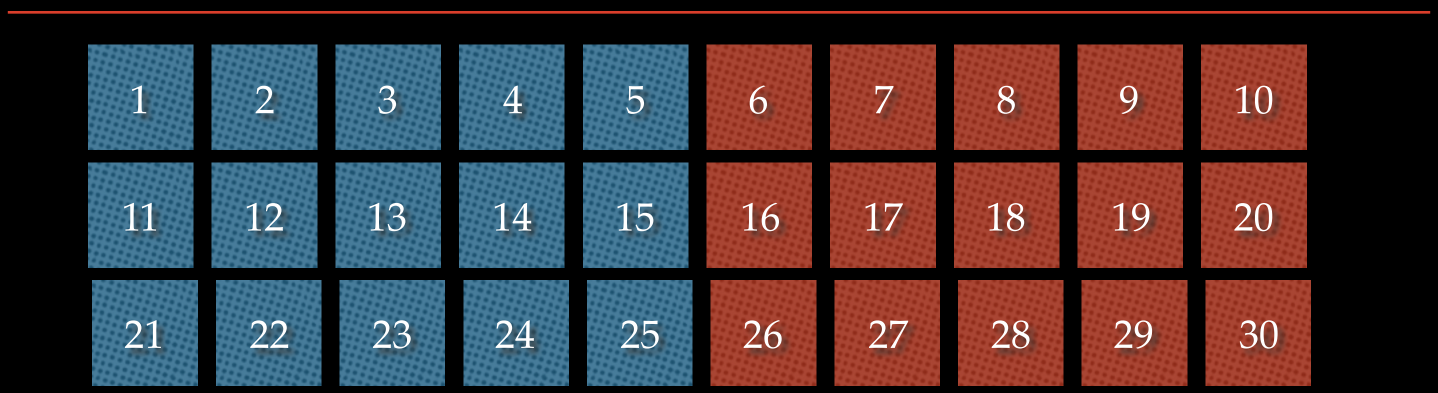

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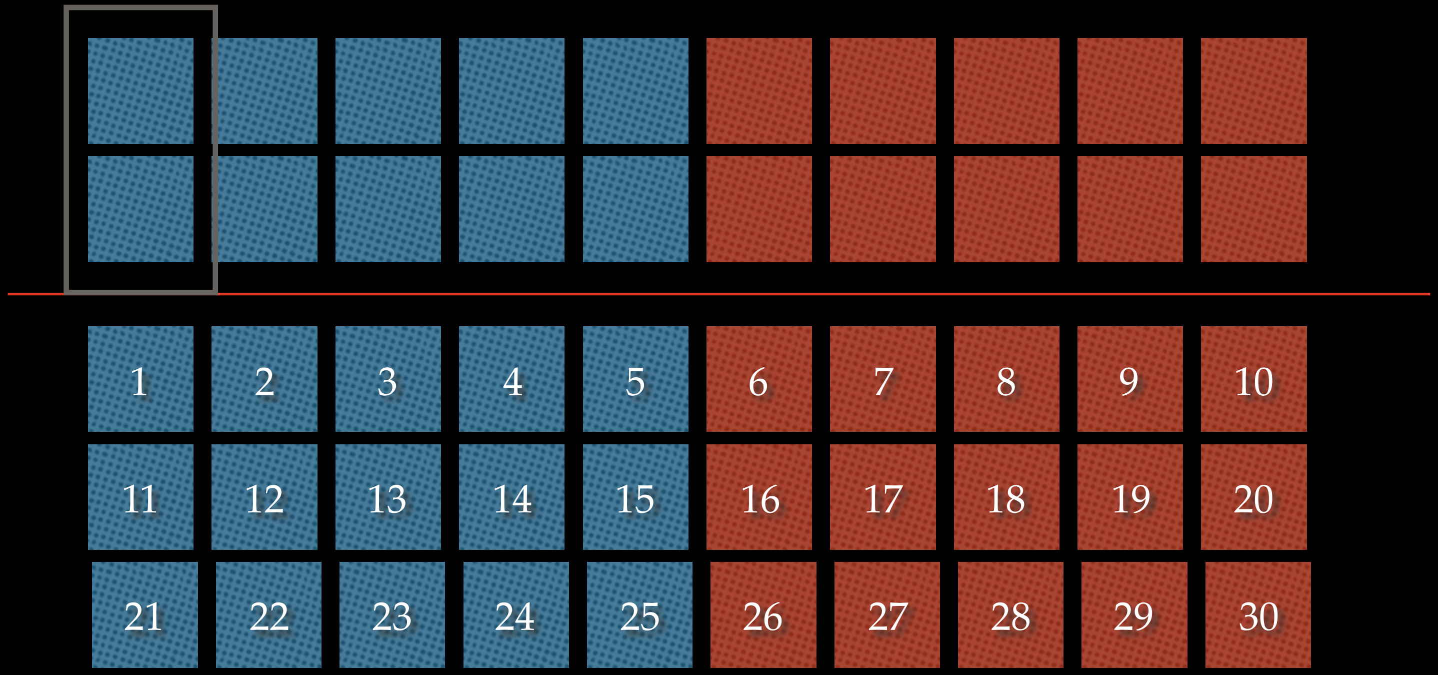

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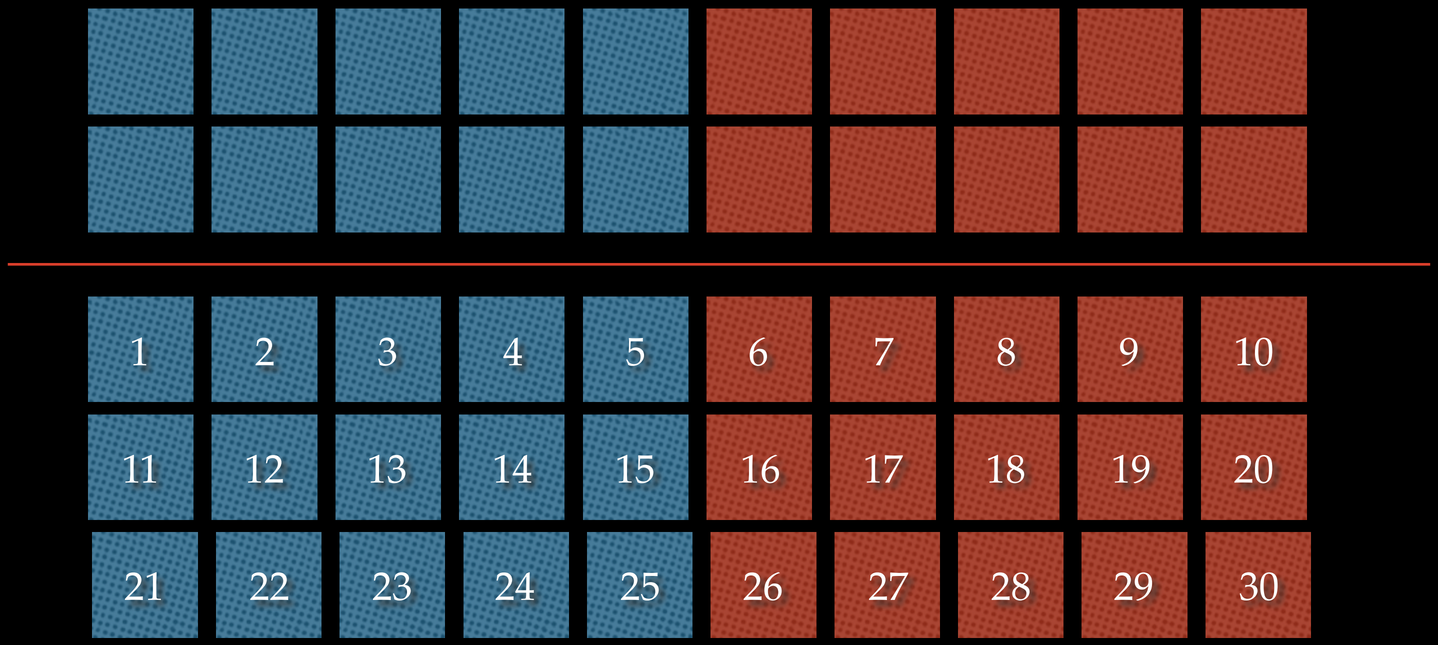

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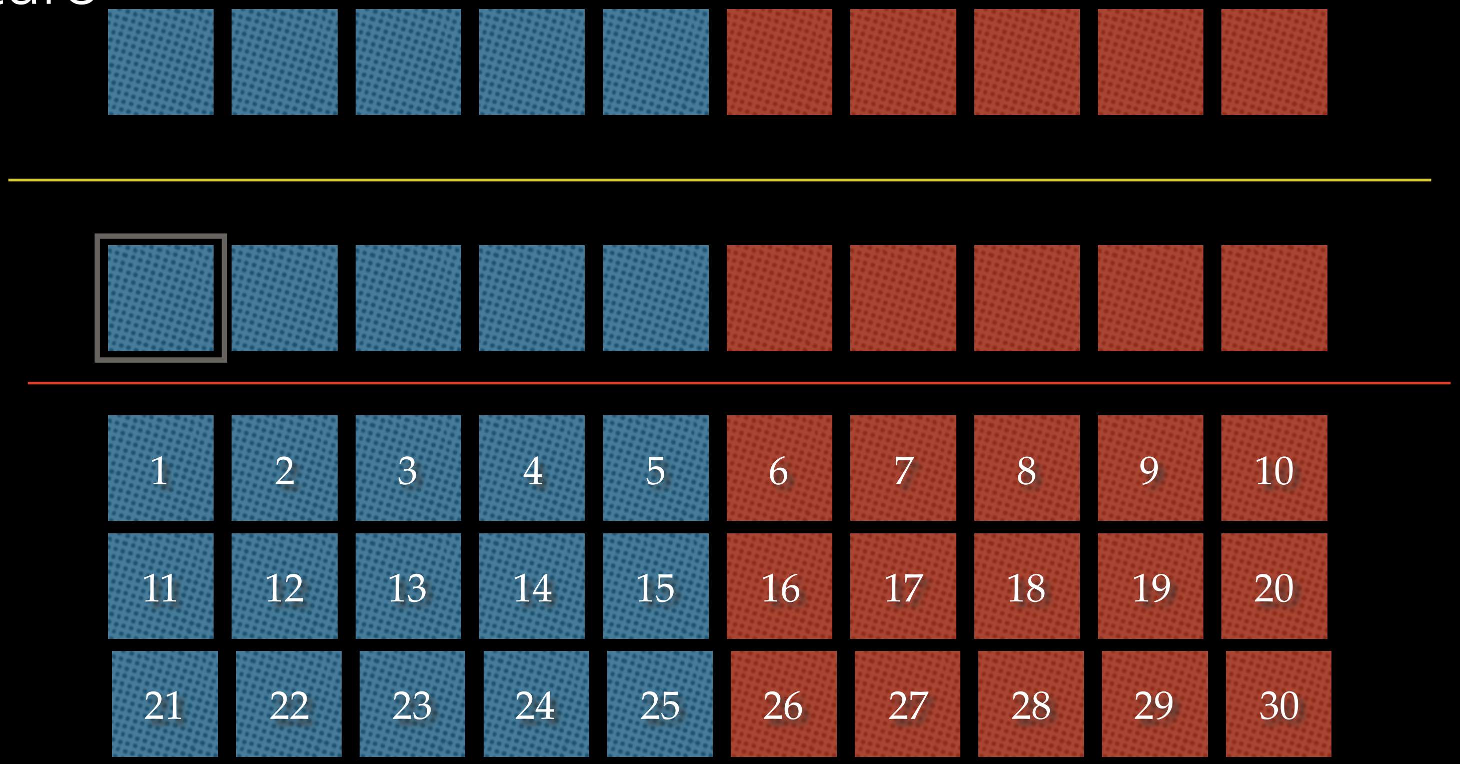

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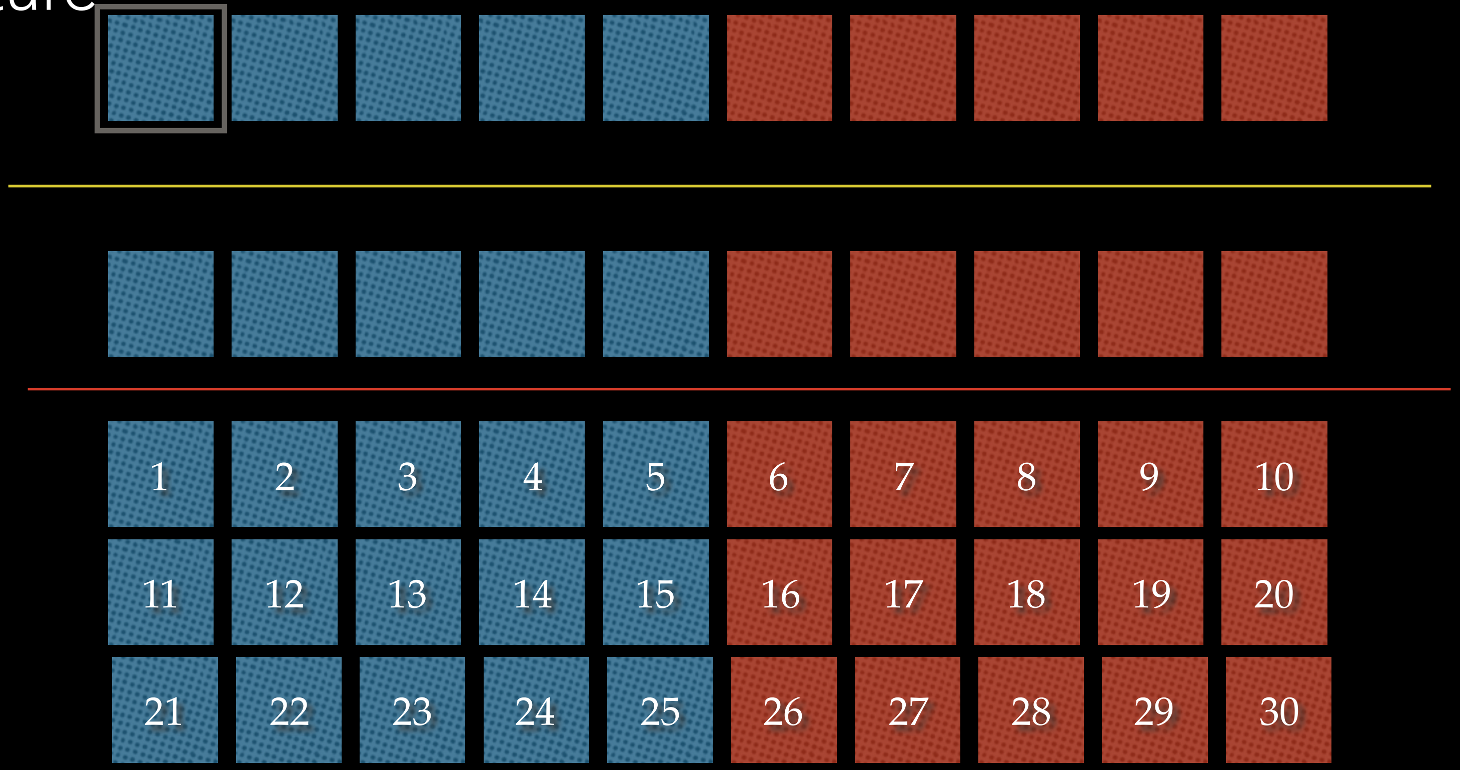

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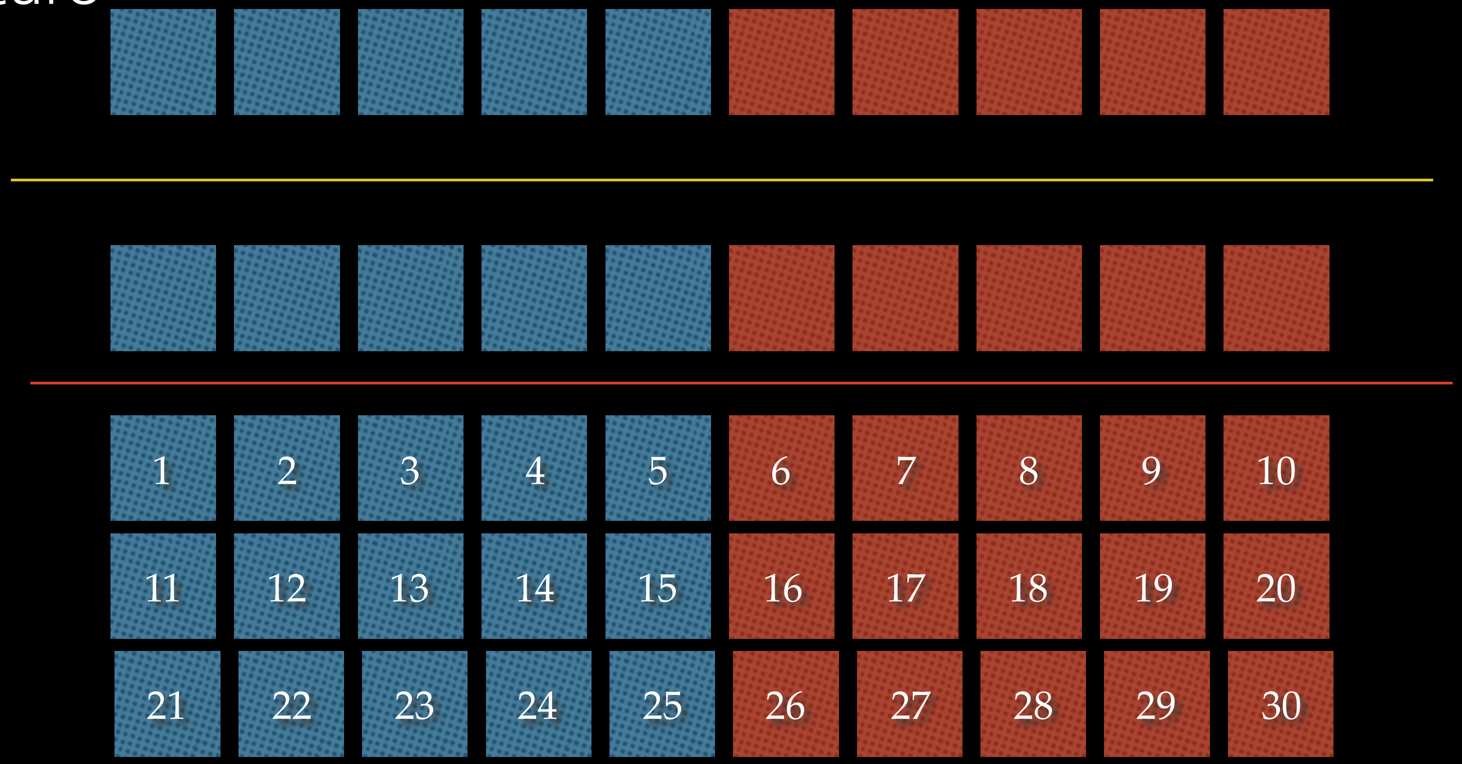

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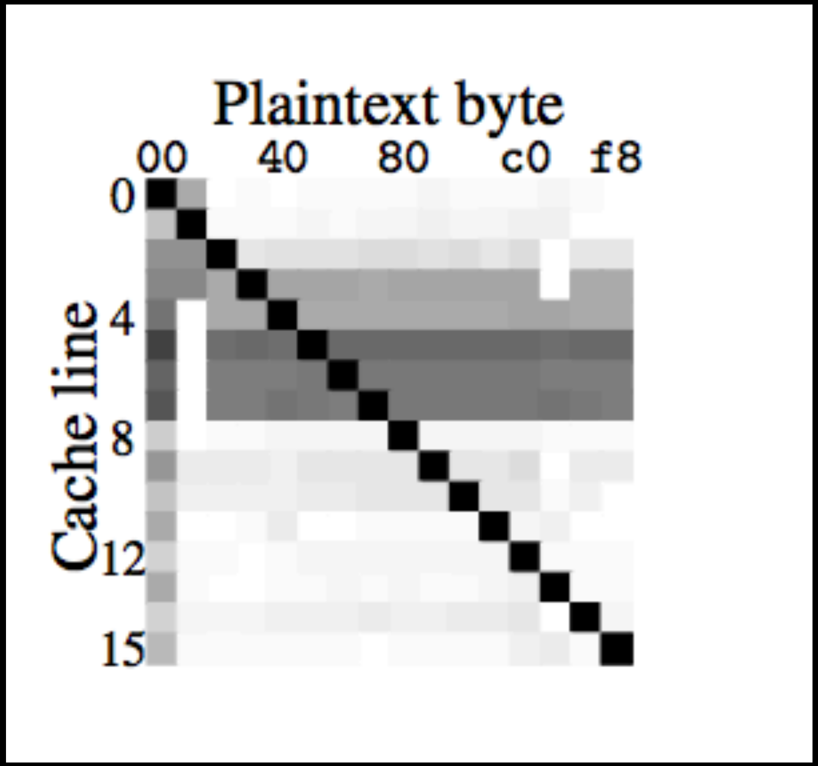

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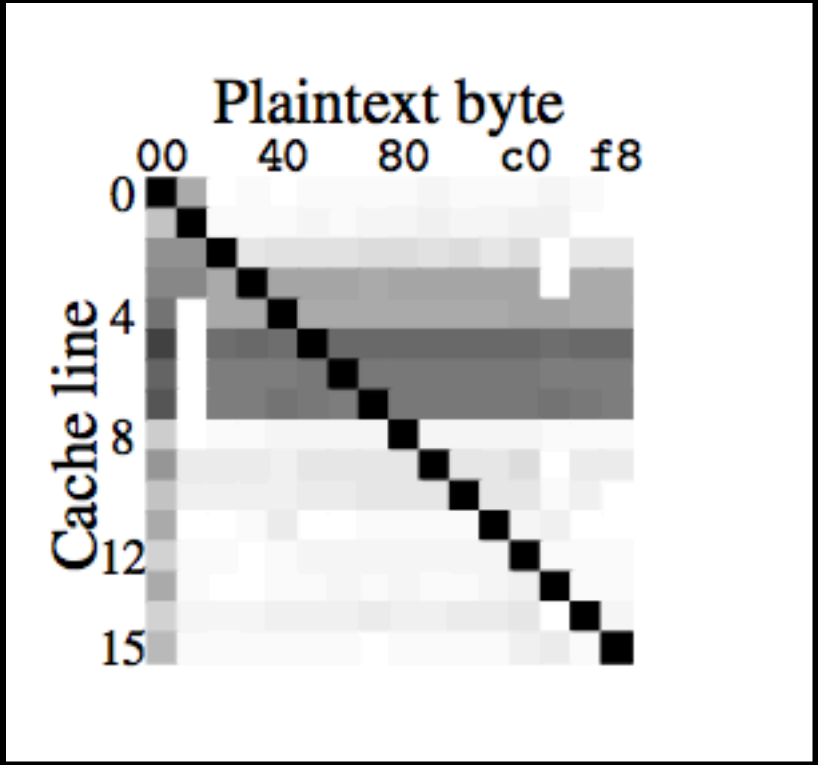
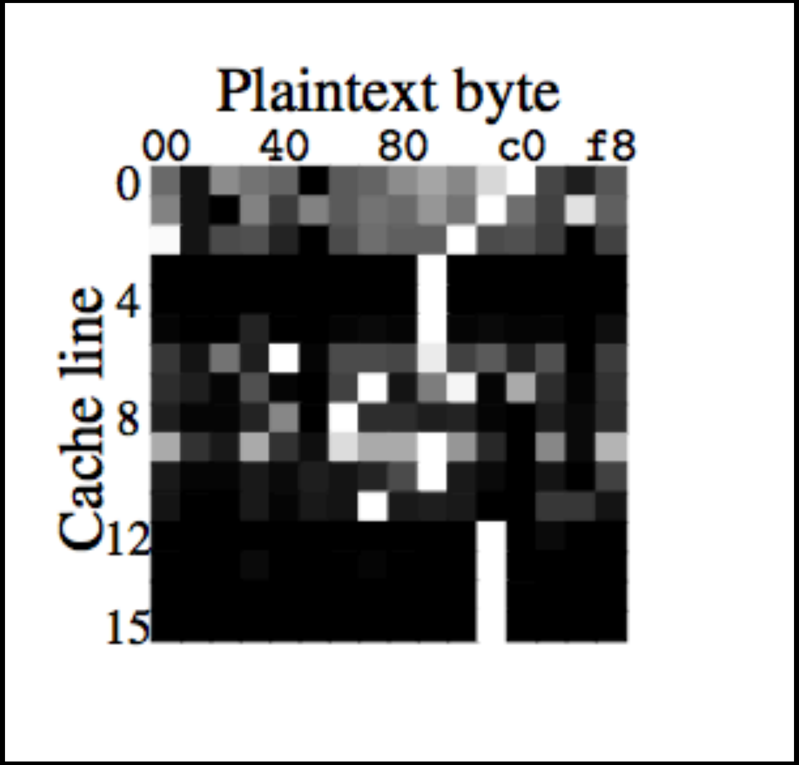
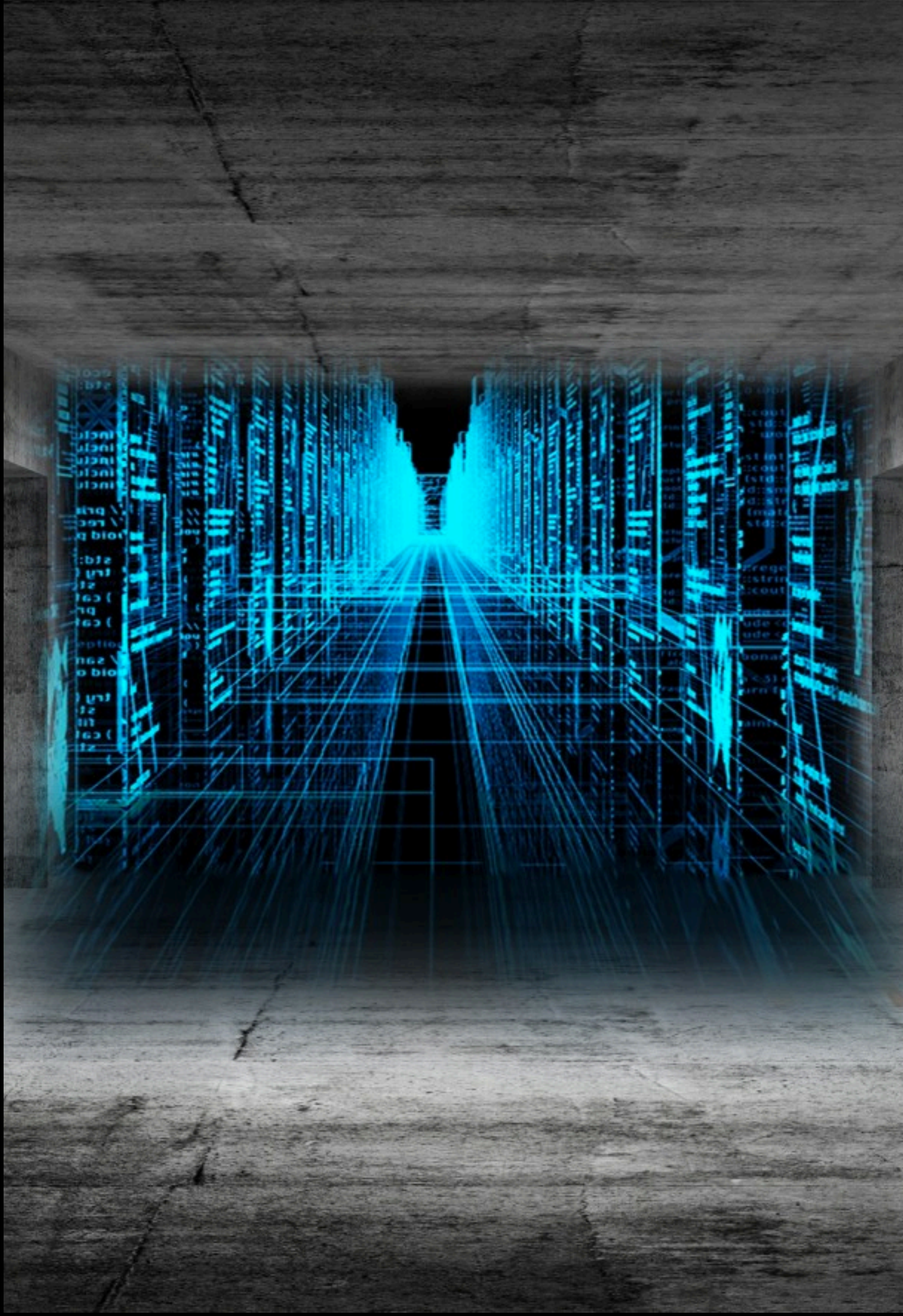




TLBLEED



TLBLEED: TLB AS SHARED STATE

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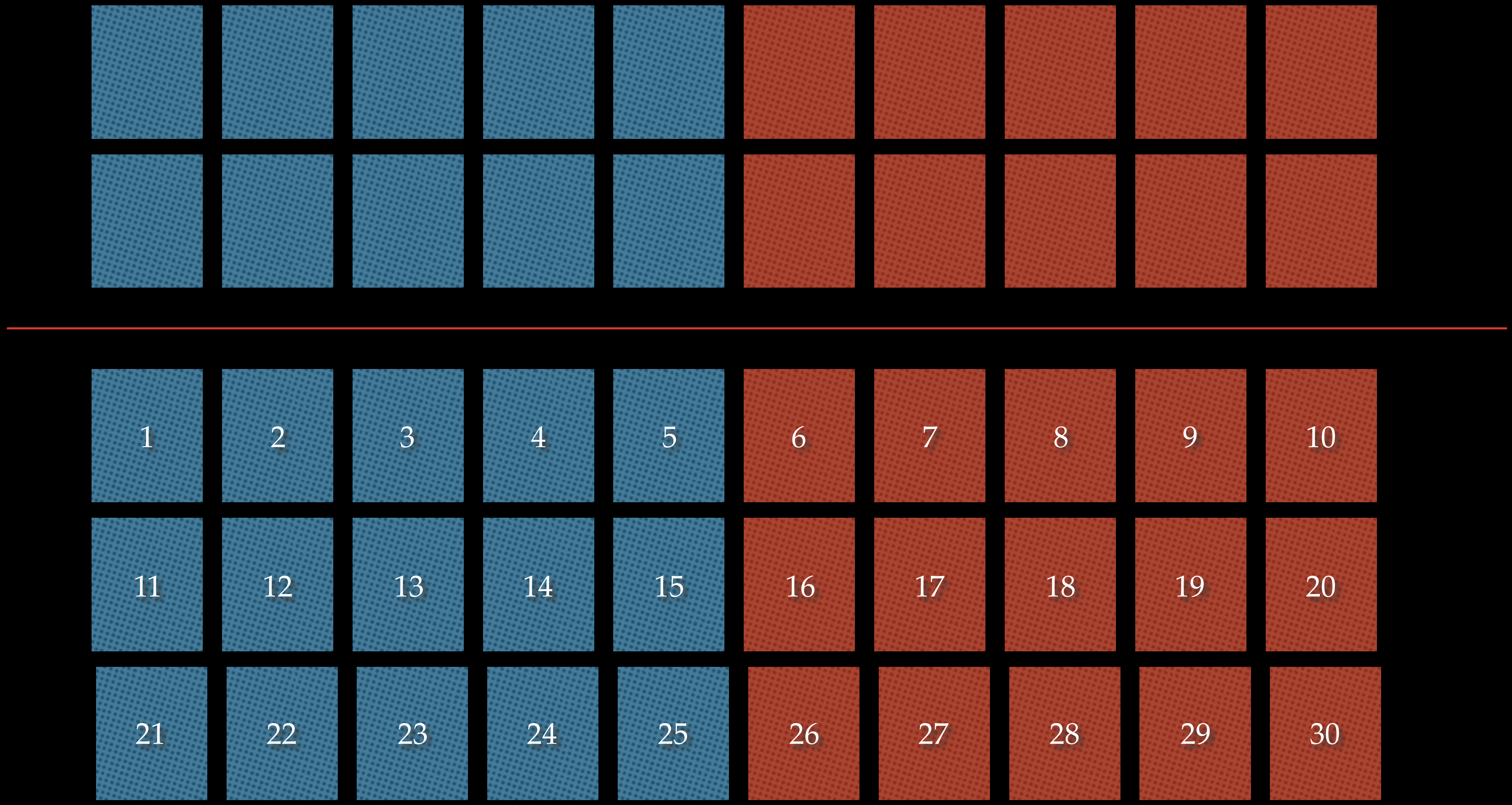
- Other structures than cache shared between threads?
- What about the TLB?
- Documented: TLB has L1iTLB, L1dTLB, and L2TLB
- They have sets and ways
- Not documented: structure

TLB IS JUST ANOTHER CACHE



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- Let’s experiment with performance counters
- Try linear structure first
- All combinations of ways (set size) and sets (stride)
- Smallest number of ways is it
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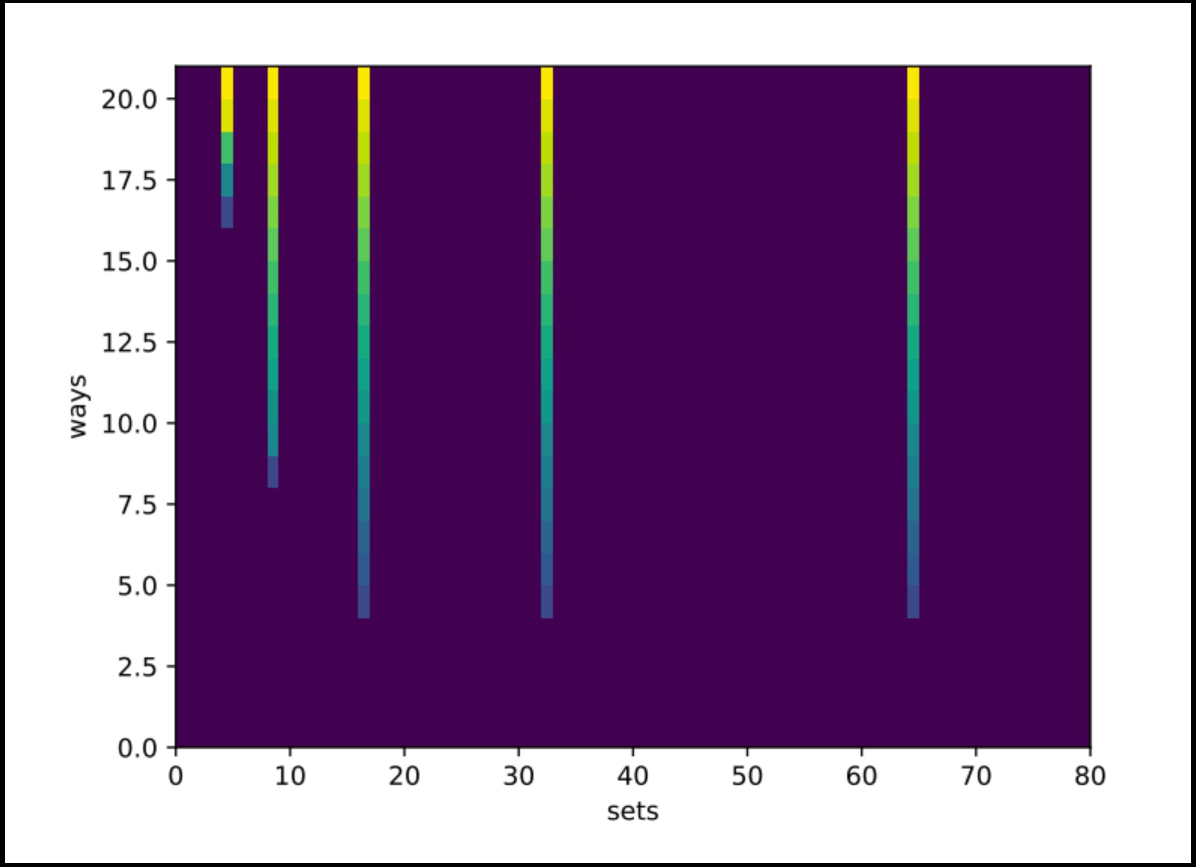

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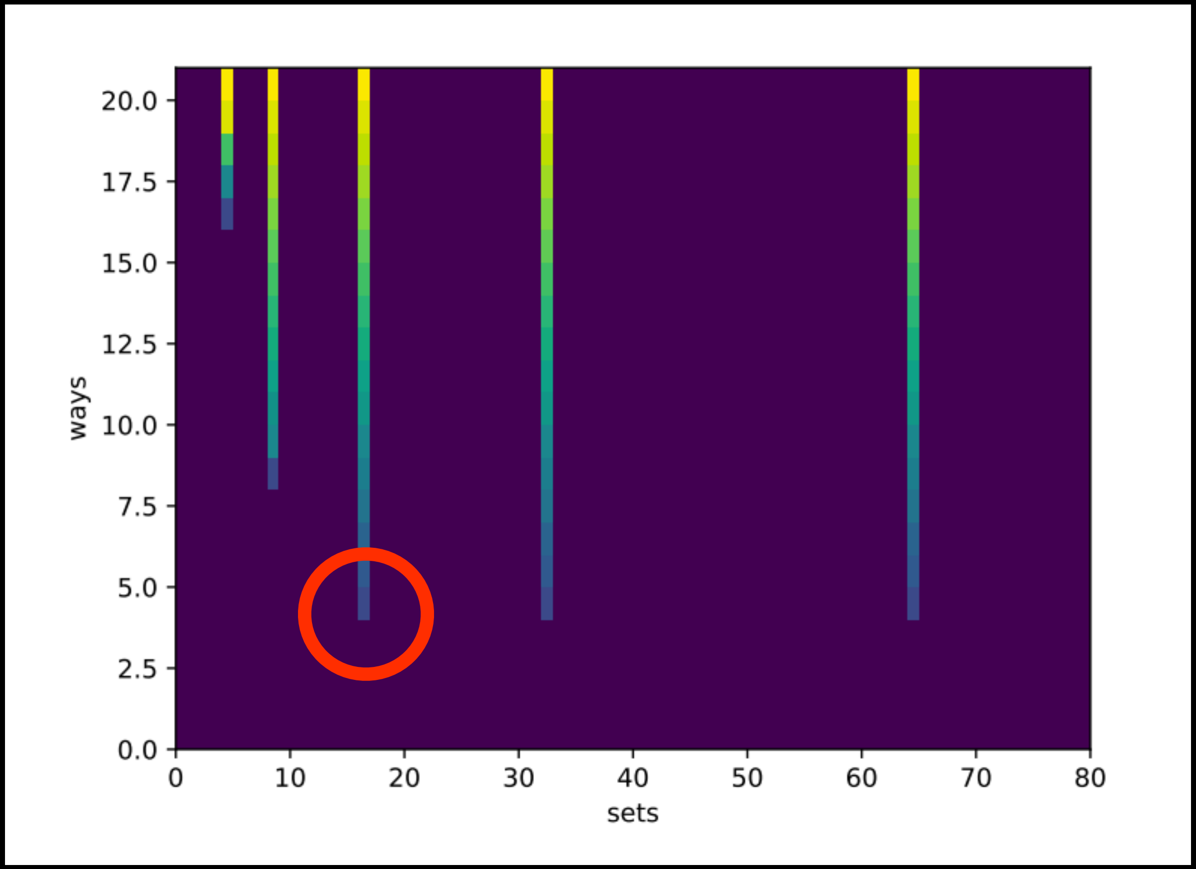

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- Represented by this matrix, using modulo 2 arithmetic

$$H = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

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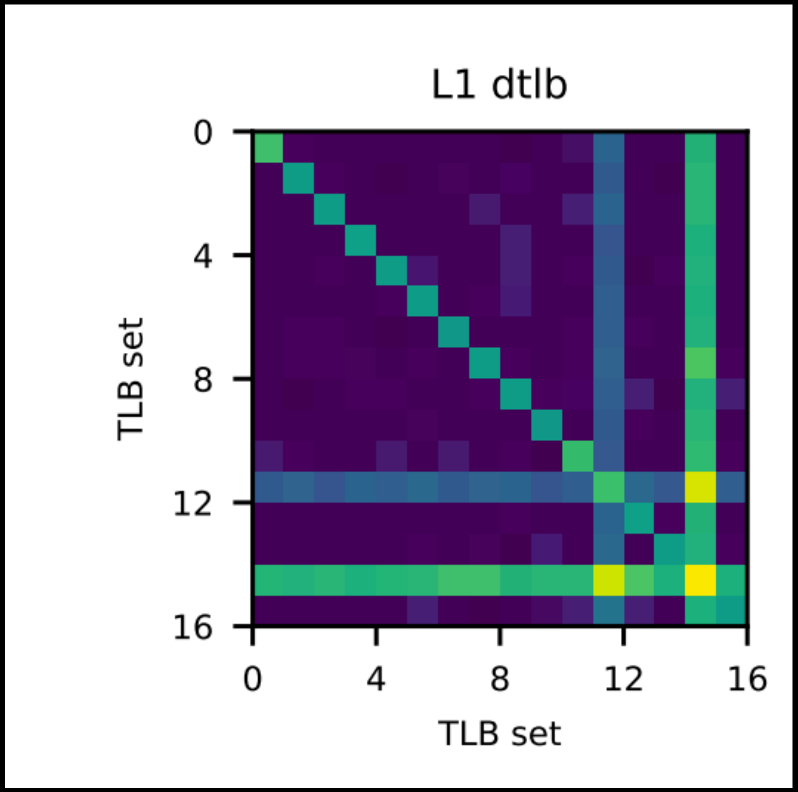

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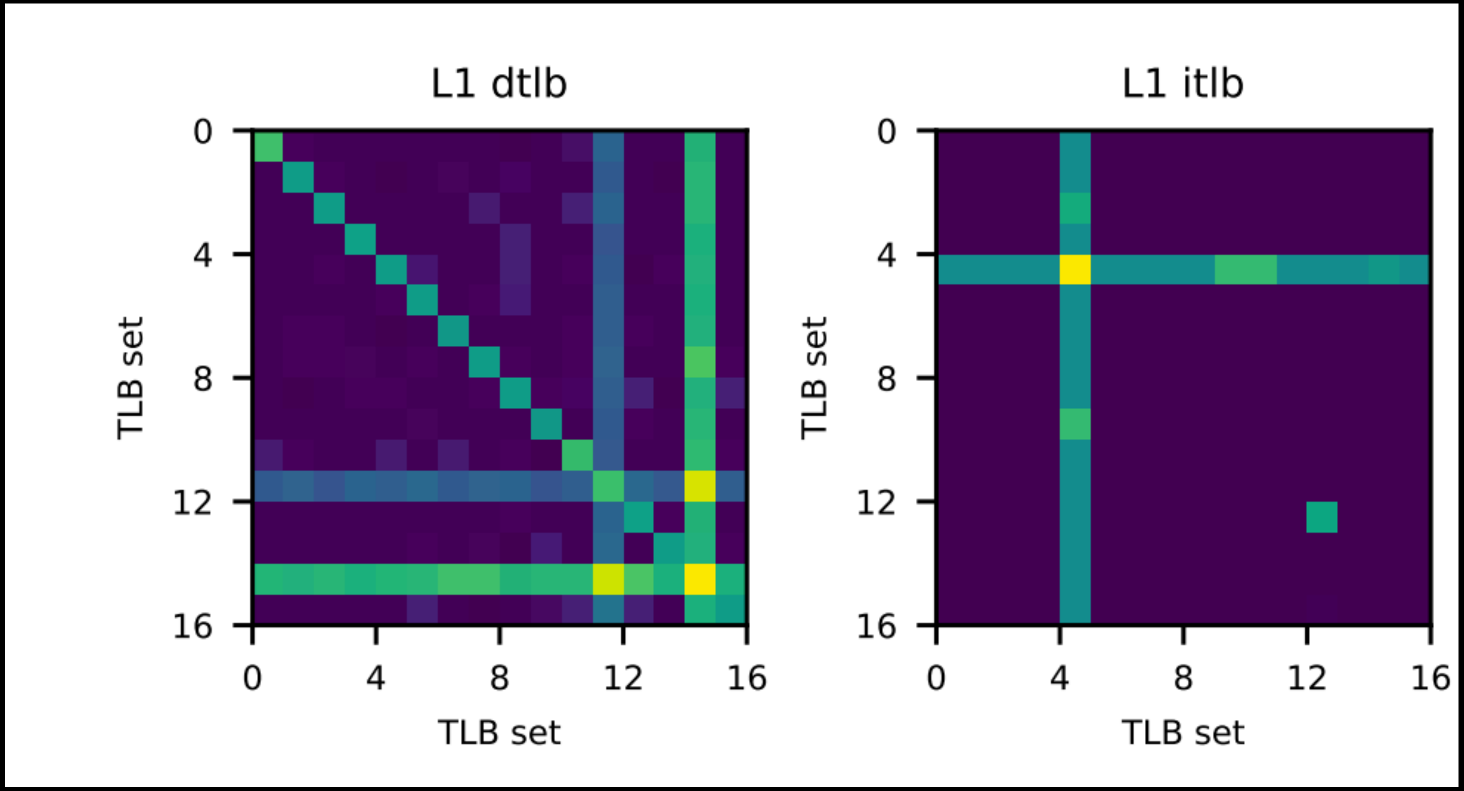

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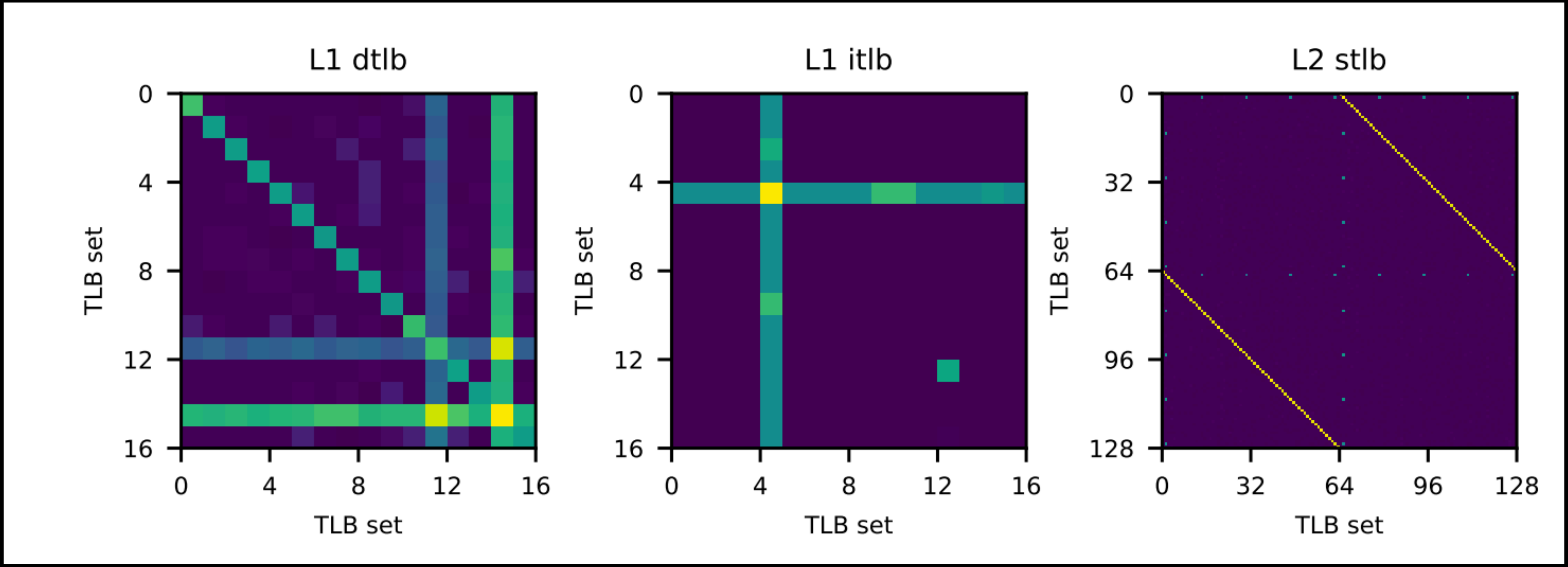

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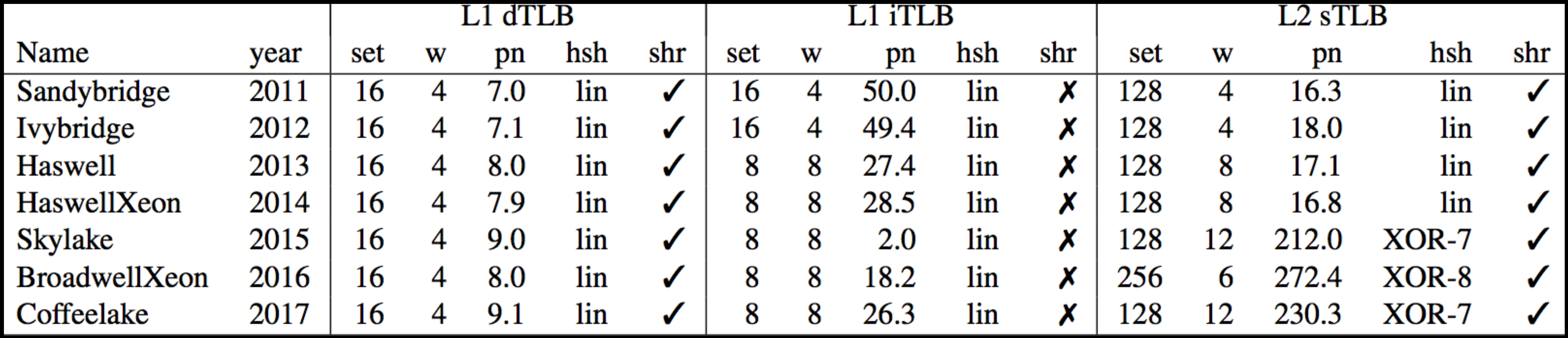

		L1 dTLB					L1 iTLB					L2 sTLB				
Name	year	set	w	pn	hsh	shr	set	w	pn	hsh	shr	set	w	pn	hsh	shr
Sandybridge	2011	16	4	7.0	lin	✓	16	4	50.0	lin	✗	128	4	16.3	lin	✓
Ivybridge	2012	16	4	7.1	lin	✓	16	4	49.4	lin	✗	128	4	18.0	lin	✓
Haswell	2013	16	4	8.0	lin	✓	8	8	27.4	lin	✗	128	8	17.1	lin	✓
HaswellXeon	2014	16	4	7.9	lin	✓	8	8	28.5	lin	✗	128	8	16.8	lin	✓
Skylake	2015	16	4	9.0	lin	✓	8	8	2.0	lin	✗	128	12	212.0	XOR-7	✓
BroadwellXeon	2016	16	4	8.0	lin	✓	8	8	18.2	lin	✗	256	6	272.4	XOR-8	✓
Coffeelake	2017	16	4	9.1	lin	✓	8	8	26.3	lin	✗	128	12	230.3	XOR-7	✓

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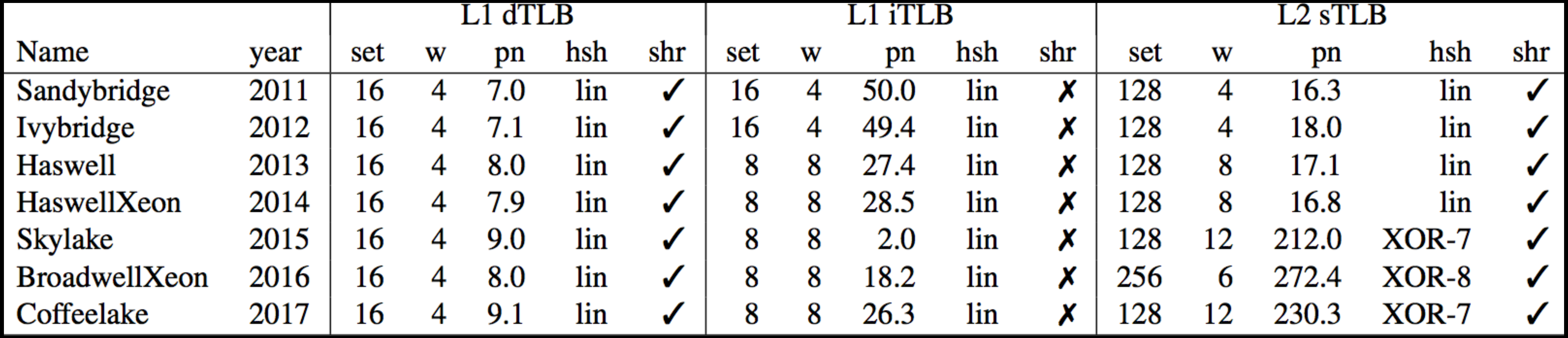
- We find more TLB properties
- Size, structure, sharing, miss penalty, hash function



		L1 dTLB					L1 iTLB					L2 sTLB				
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Ivybridge	2012	16	4	7.1	lin	✓	16	4	49.4	lin	✗	128	4	18.0	lin	✓
Haswell	2013	16	4	8.0	lin	✓	8	8	27.4	lin	✗	128	8	17.1	lin	✓
HaswellXeon	2014	16	4	7.9	lin	✓	8	8	28.5	lin	✗	128	8	16.8	lin	✓
Skylake	2015	16	4	9.0	lin	✓	8	8	2.0	lin	✗	128	12	212.0	XOR-7	✓
BroadwellXeon	2016	16	4	8.0	lin	✓	8	8	18.2	lin	✗	256	6	272.4	XOR-8	✓
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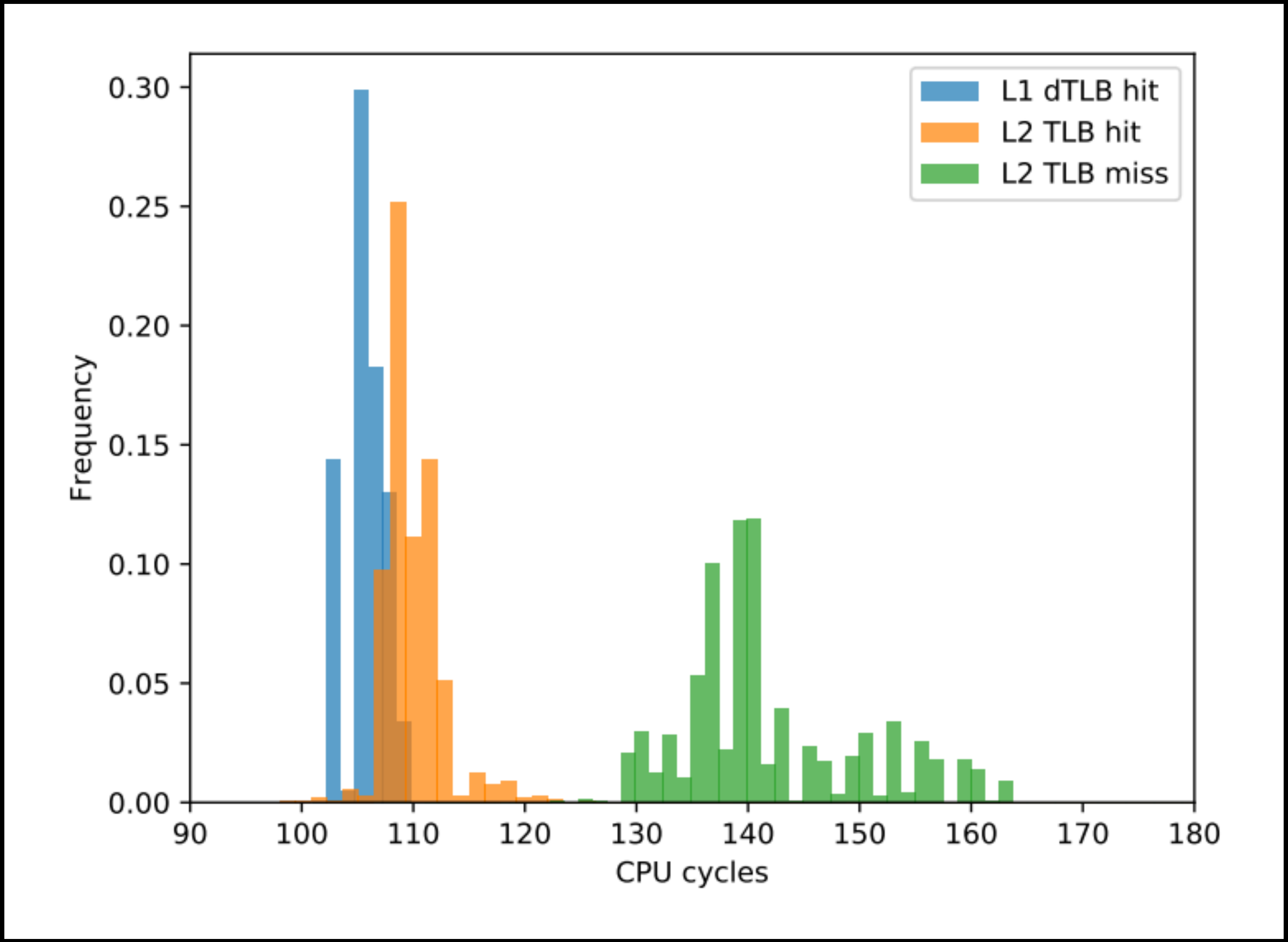

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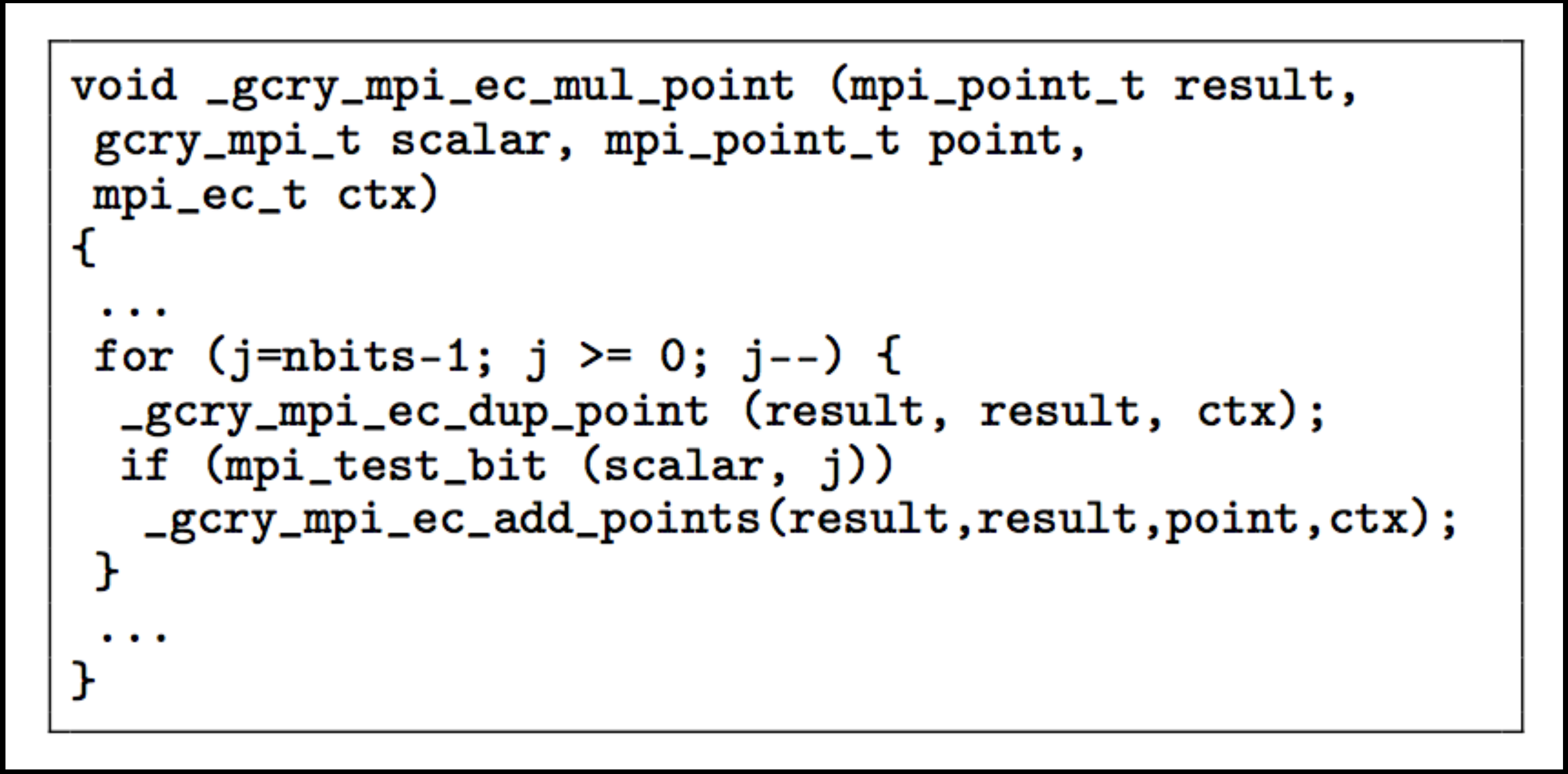
- Let’s observe EdDSA ECC key multiplication



```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
 gcry_mpi_t scalar, mpi_point_t point,
 mpi_ec_t ctx)
{
 ...
 for (j=nbits-1; j >= 0; j--) {
  _gcry_mpi_ec_dup_point (result, result, ctx);
  if (mpi_test_bit (scalar, j))
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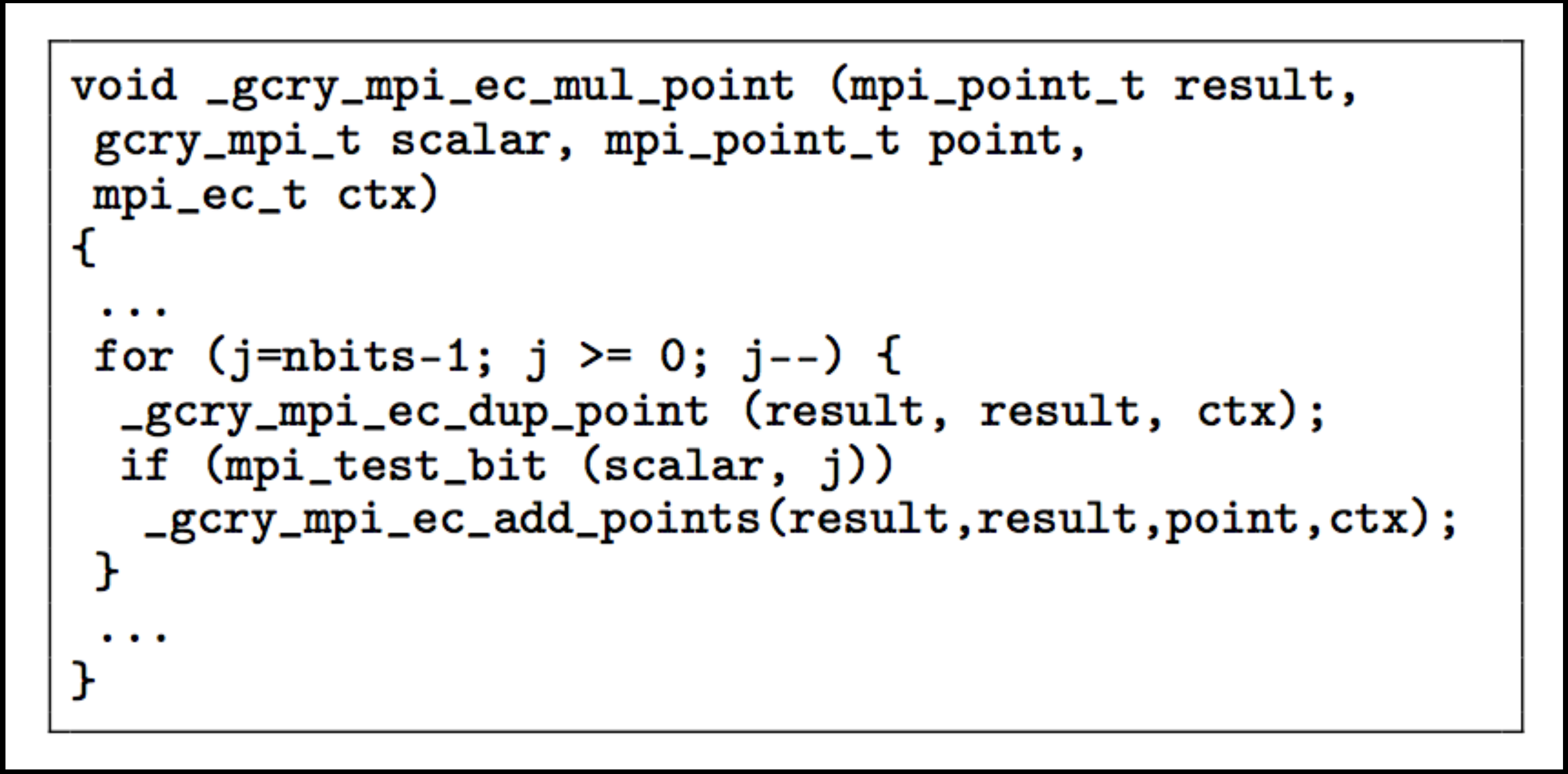

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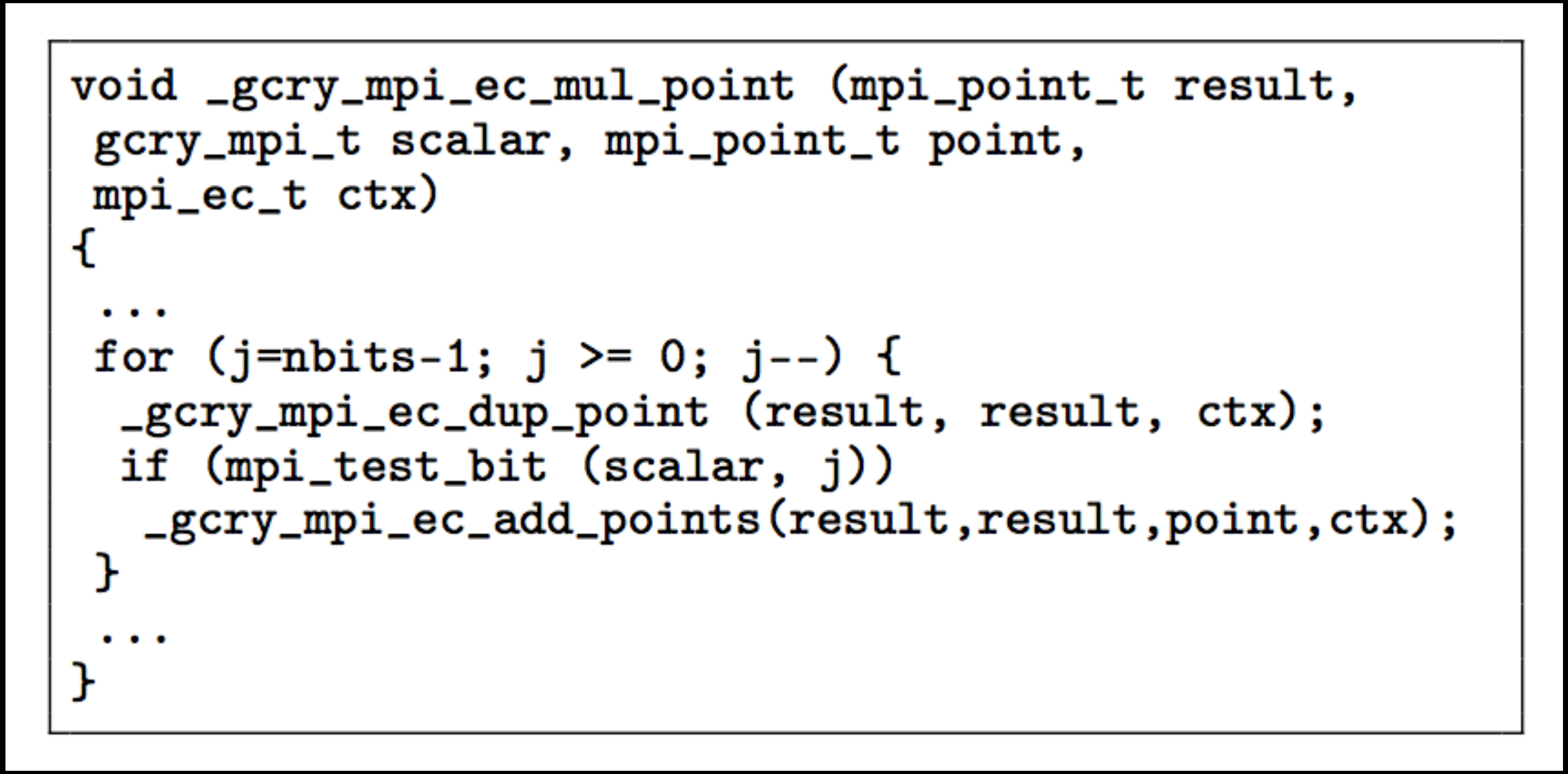
- But: we can not use code information! Only data..!



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- Too much activity in both blue/green cases

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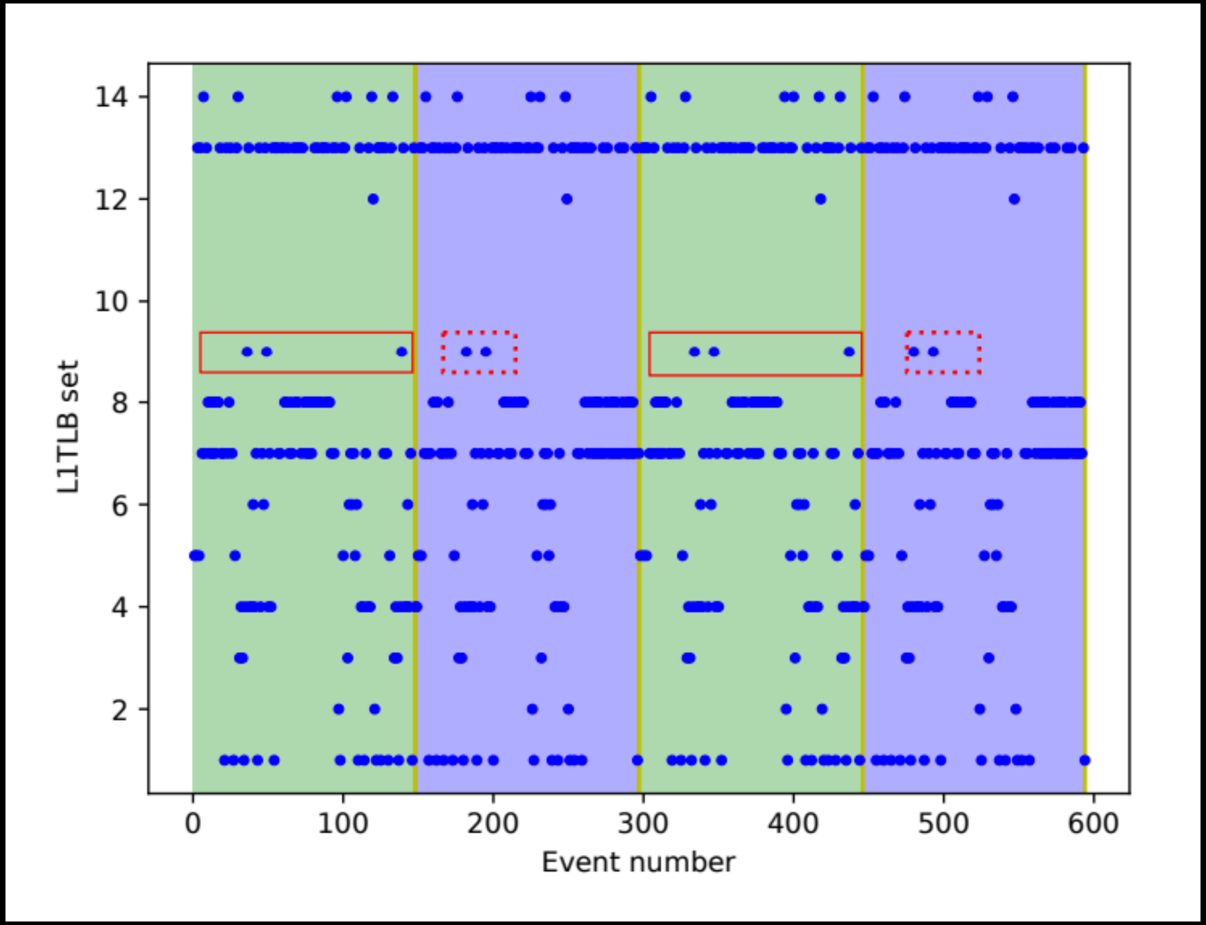

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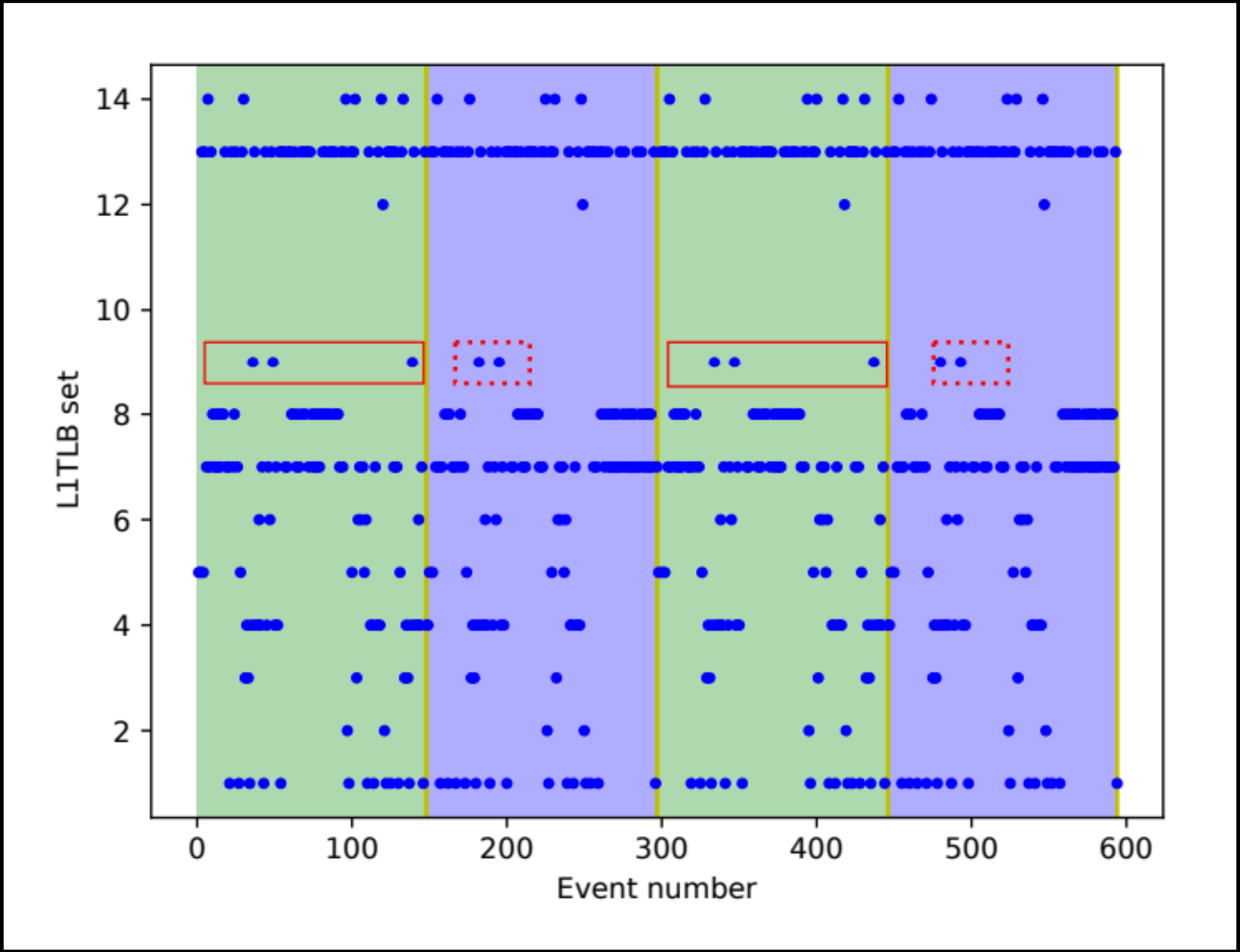

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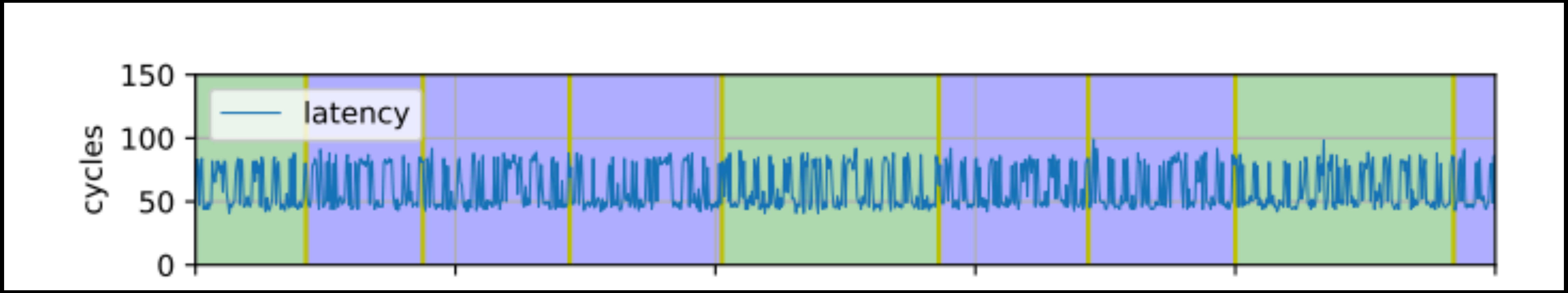

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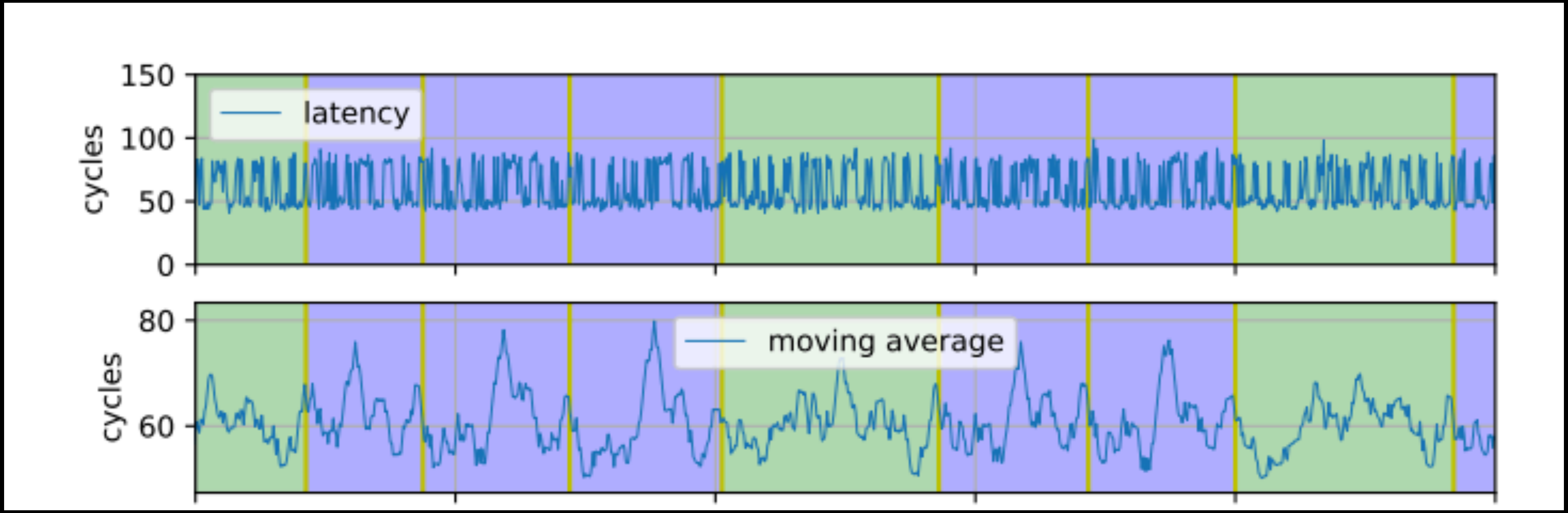

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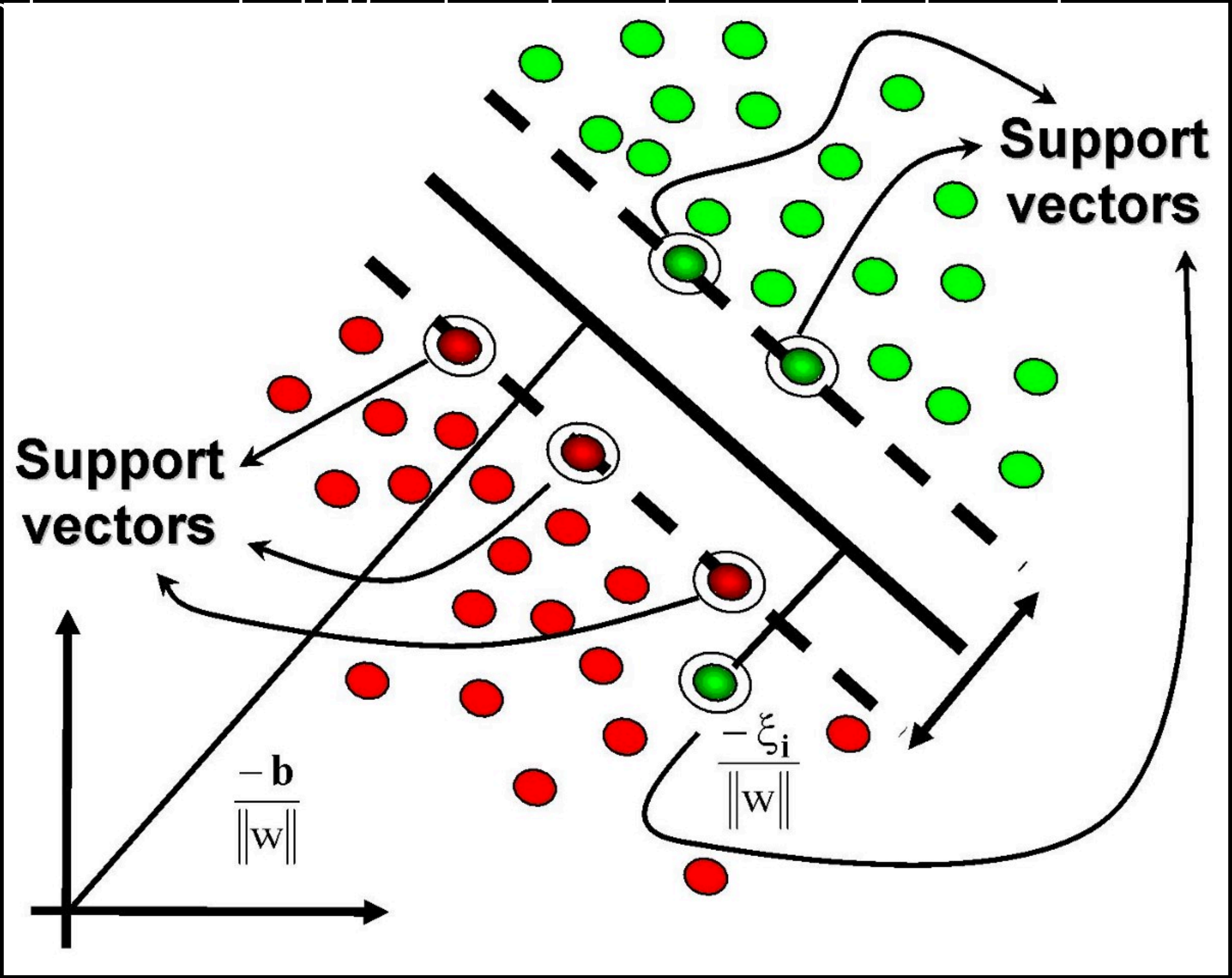

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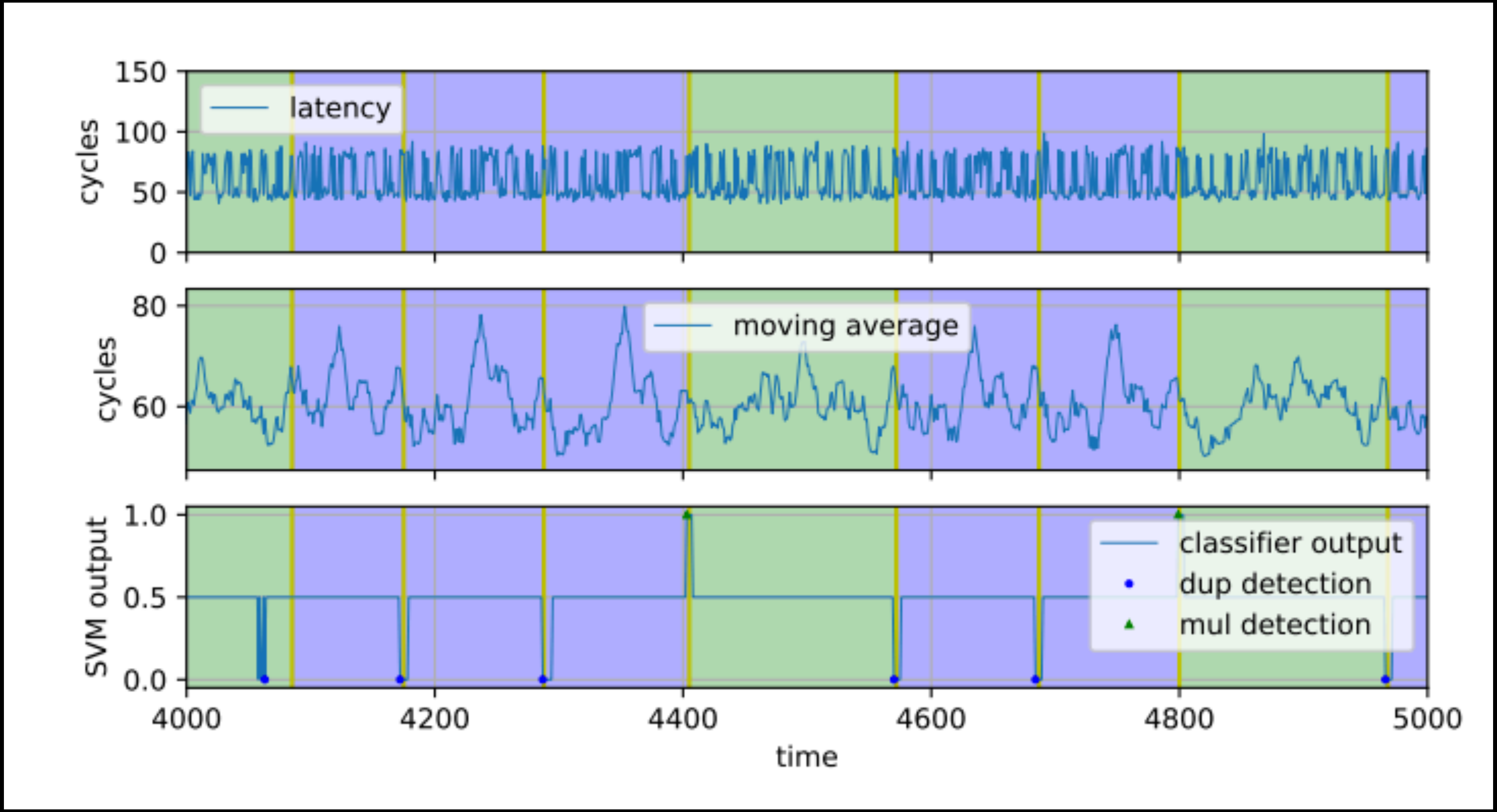

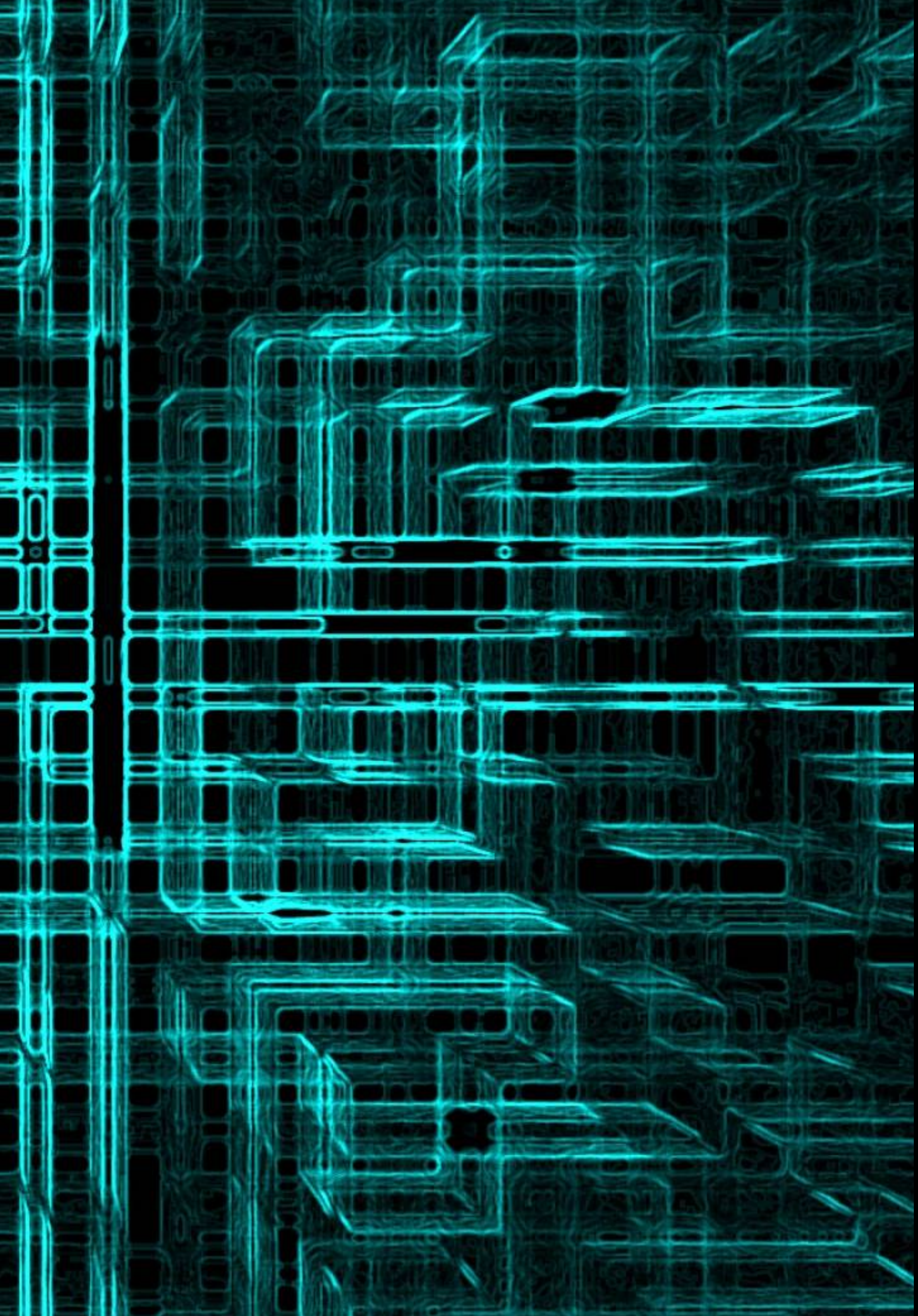

EVALUATION

TLBLEED RELIABILITY

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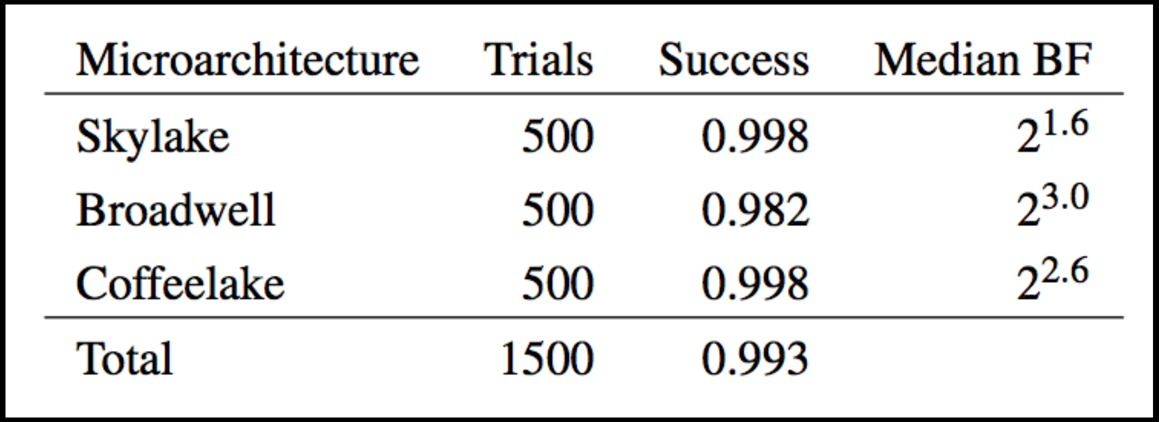
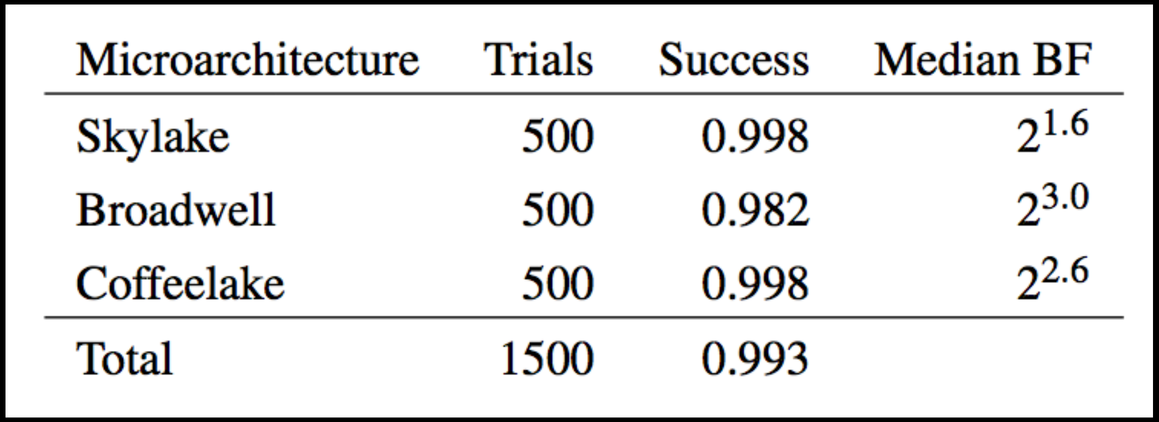


Microarchitecture	Trials	Success	Median BF
Skylake	500	0.998	$2^{1.6}$
Broadwell	500	0.982	$2^{3.0}$
Coffeelake	500	0.998	$2^{2.6}$
Total	1500	0.993	

TLBLEED RELIABILITY



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- Median end-to-end time: 17s

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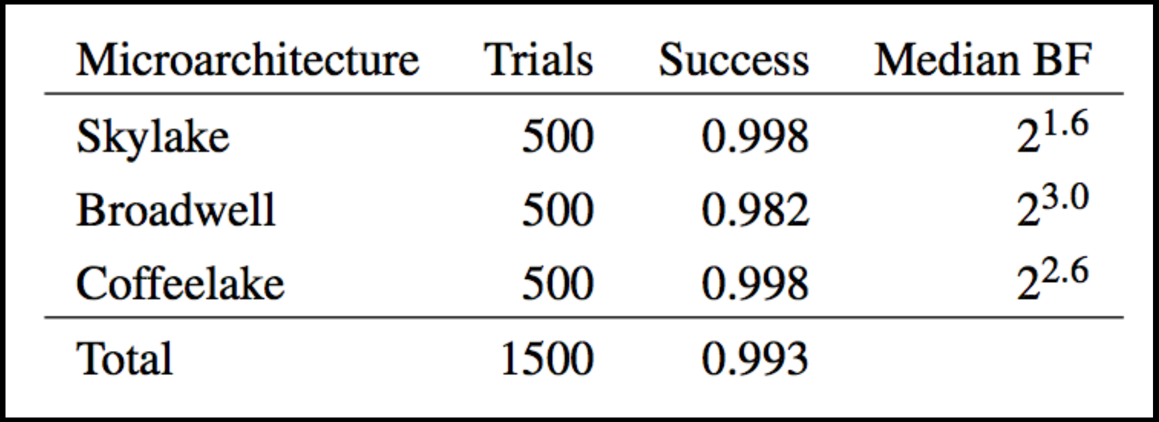

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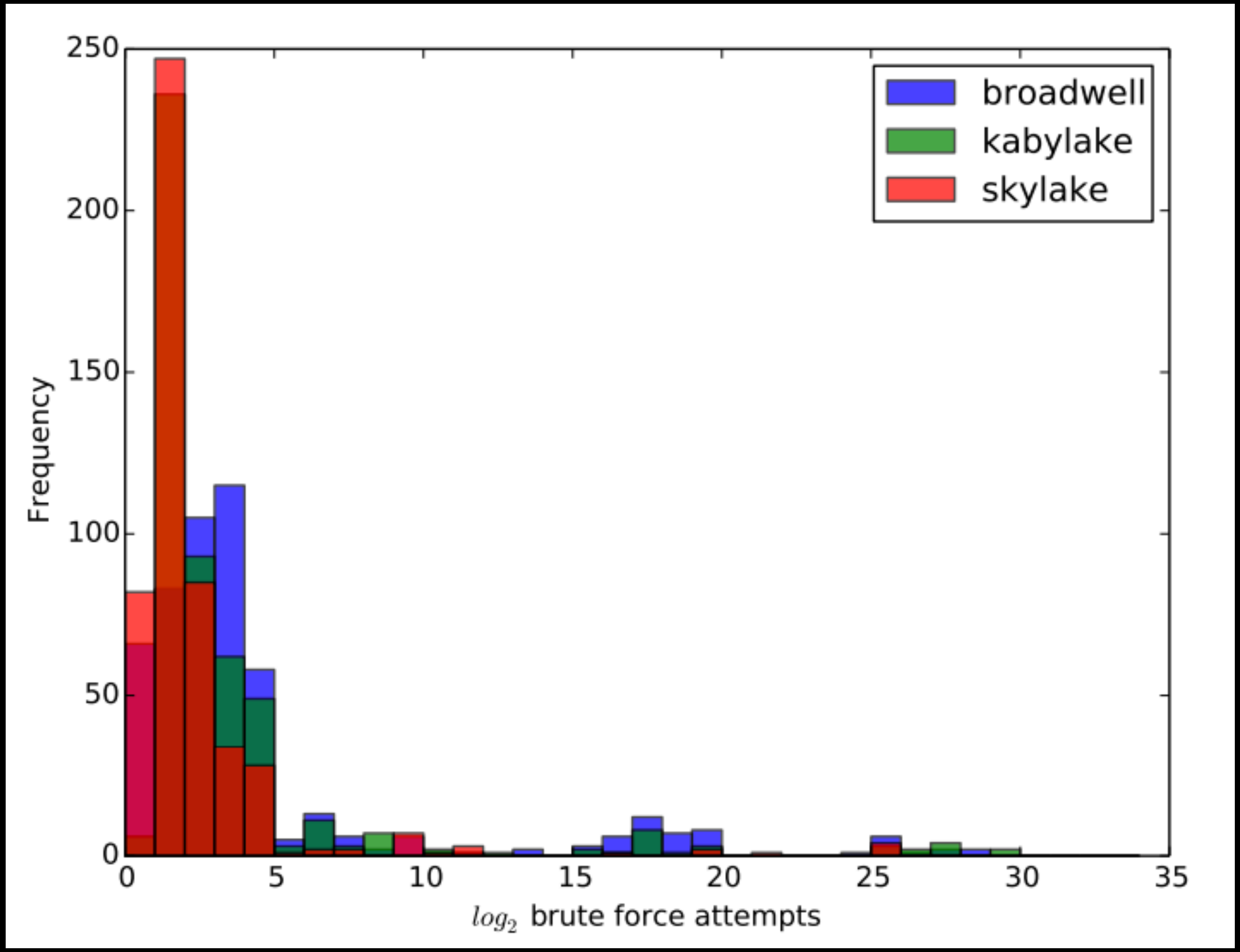

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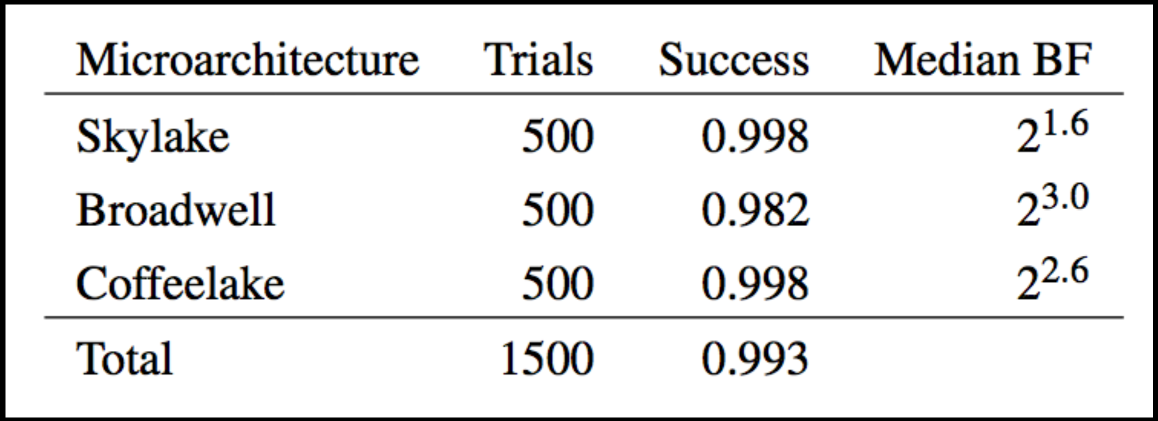

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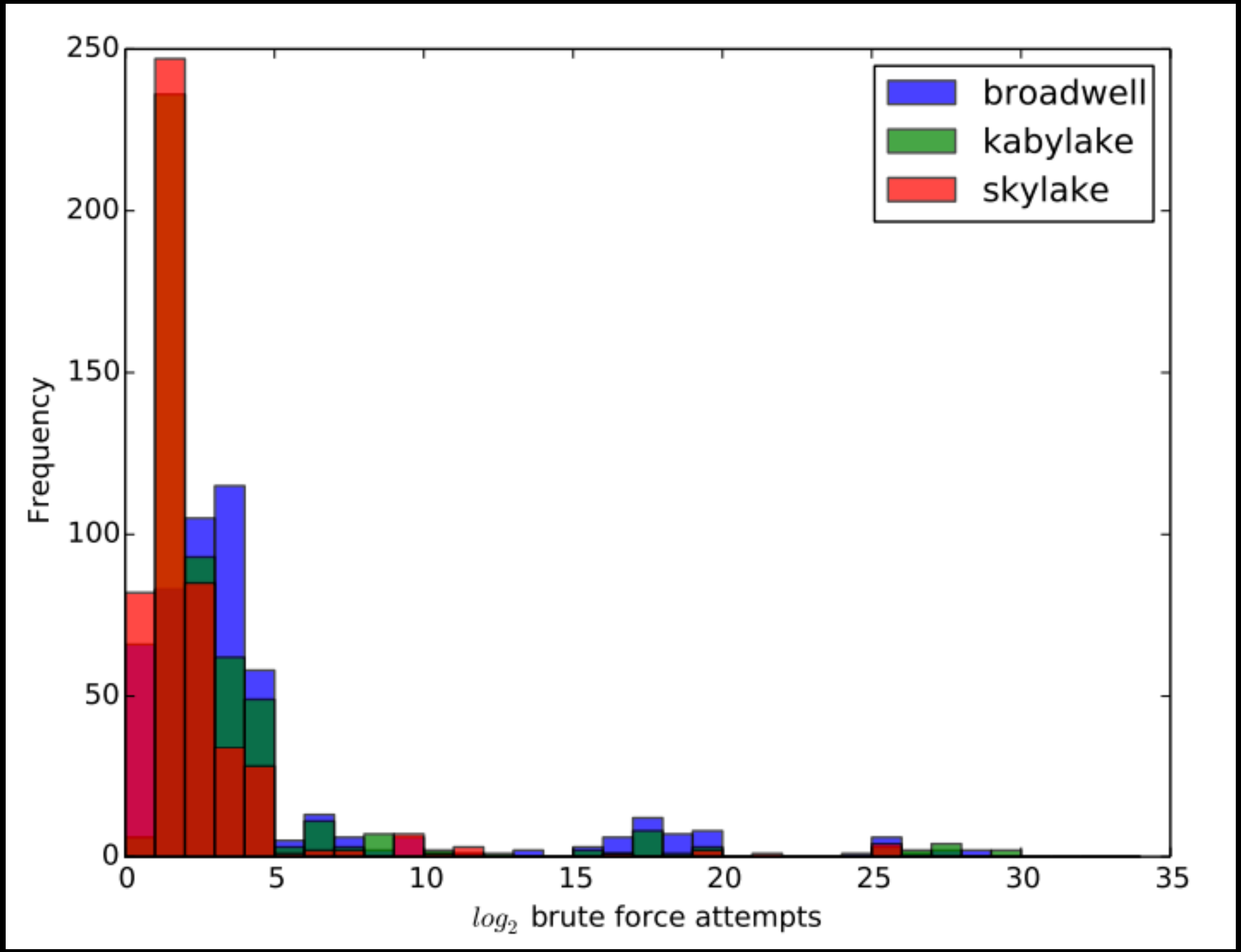

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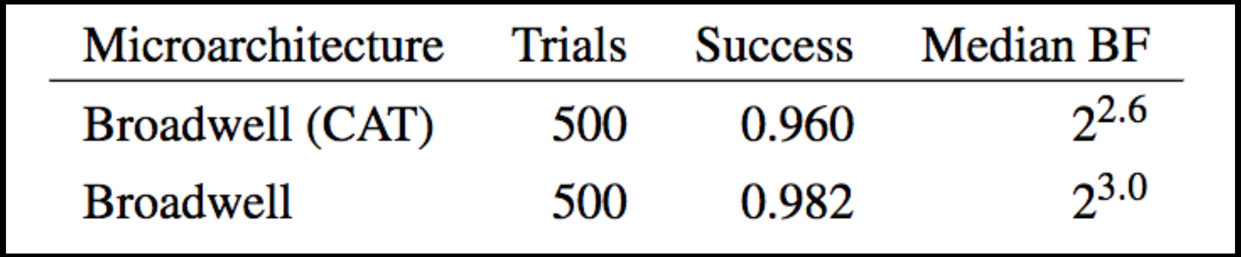

Microarchitecture	Trials	Success	Median BF
Broadwell (CAT)	500	0.960	$2^{2.6}$
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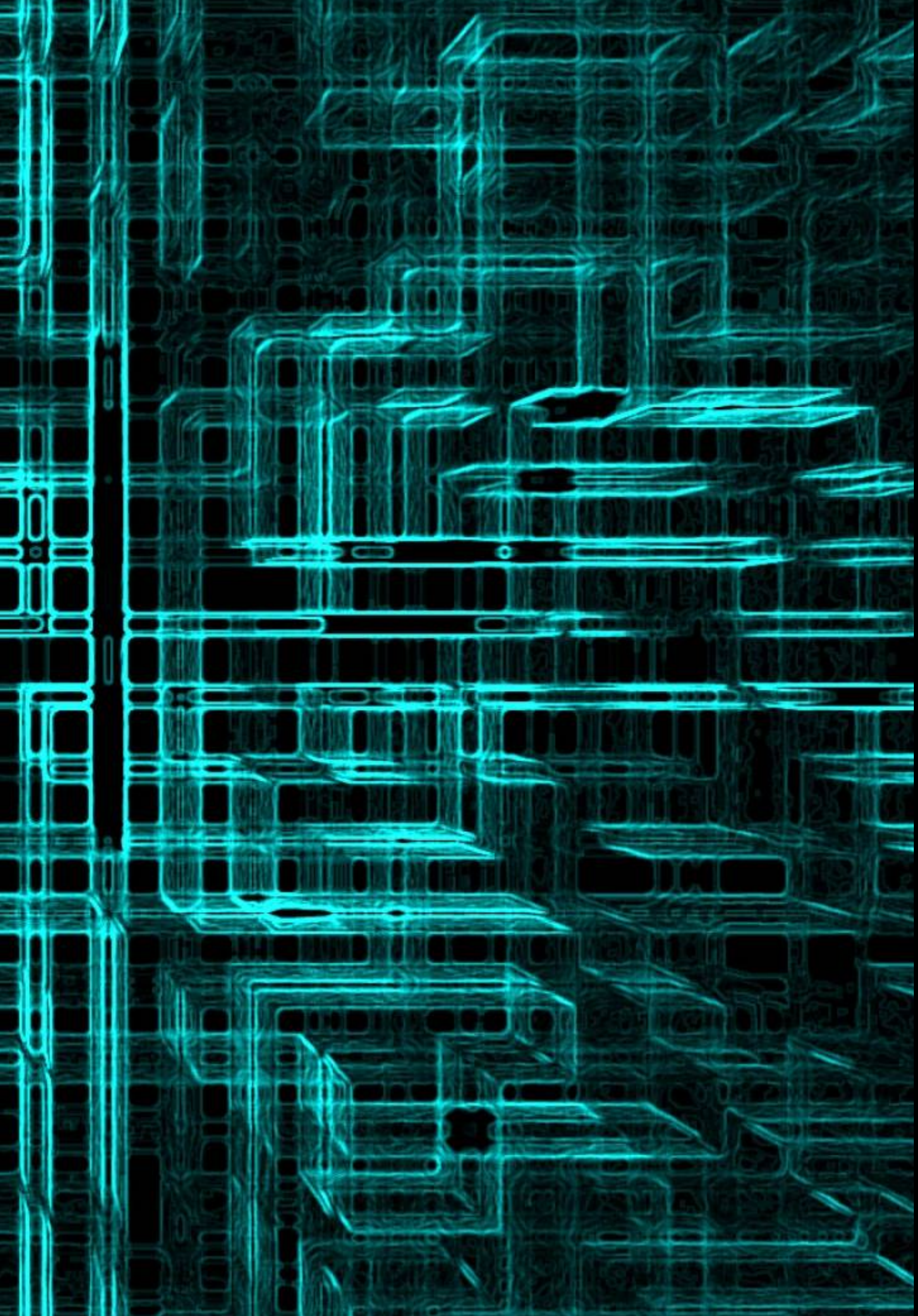

RECEPTION

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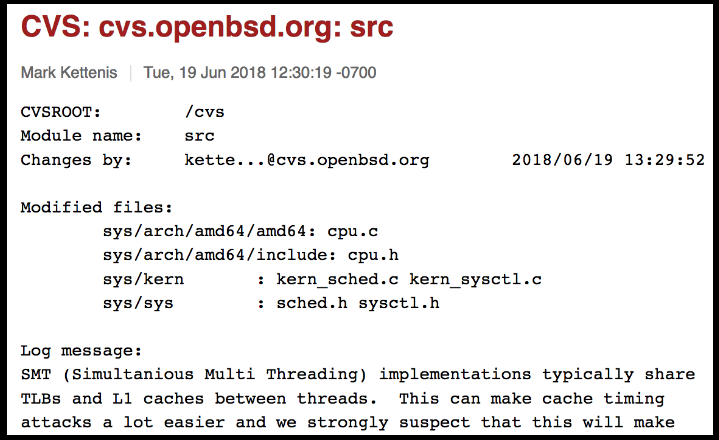

CVS: cvs.openbsd.org: src

Mark Kettenis | Tue, 19 Jun 2018 12:30:19 -0700

```
CVSROOT:        /cvs
Module name:    src
Changes by:     kette...@cvs.openbsd.org        2018/06/19 13:29:52

Modified files:
        sys/arch/amd64/amd64: cpu.c
        sys/arch/amd64/include: cpu.h
        sys/kern        : kern_sched.c kern_sysctl.c
        sys/sys         : sched.h sysctl.h

Log message:
SMT (Simultanious Multi Threading) implementations typically share
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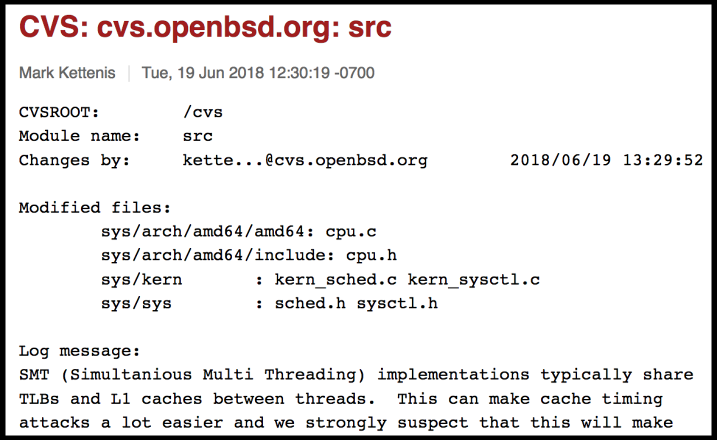

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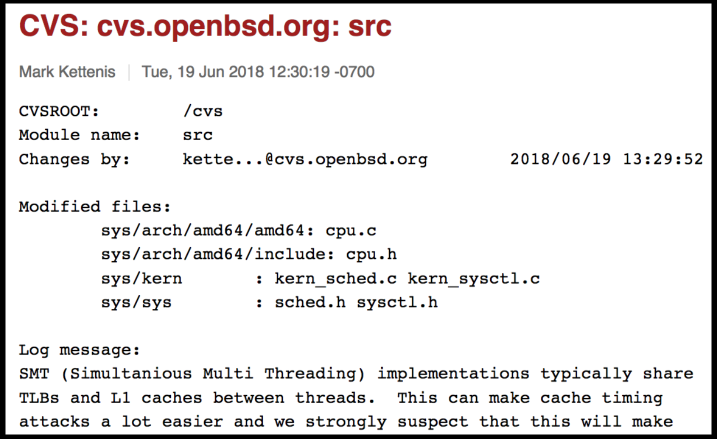

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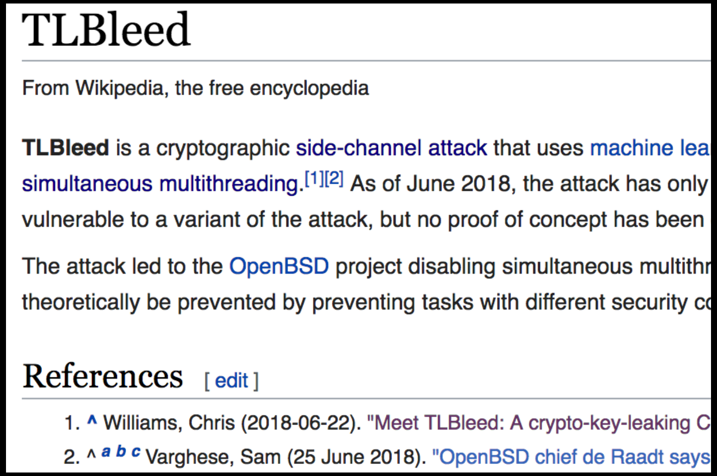

TLBleed

From Wikipedia, the free encyclopedia

TLBleed is a cryptographic side-channel attack that uses machine lea simultaneous multithreading.[1][2] As of June 2018, the attack has only vulnerable to a variant of the attack, but no proof of concept has been

The attack led to the OpenBSD project disabling simultaneous multithr theoretically be prevented by preventing tasks with different security c

References [edit]

1. ^ Williams, Chris (2018-06-22). "Meet TLBleed: A crypto-key-leaking C
2. ^ a b c Varghese, Sam (25 June 2018). "OpenBSD chief de Raadt says

CONCLUSION

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- Thank you for listening